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WARFIGHTER ADVANTAGE: SECURING AMERICA'S SEMICONDUCTOR EDGE FOR NATIONAL DEFENSE

MICROELECTRONICS INDUSTRY STUDY GROUP REPORT

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FIELD STUDY

The Microelectronics Industry Study incorporated guest speakers, domestic and international travel, as well as corporate engagement to gain insight into both the government and private sector perspectives of the semiconductor industry. Engagement included several presentations by professionals in the industry with diverse experience and points of view. Students developed a thorough understanding of U.S. efforts to fortify a leading role in the semiconductor industry. During these engagements, students examined efforts to enhance national competitiveness, redevelop the U.S.-based semiconductor supply chain, the role of public-private partnerships, and leading and bleeding-edge efforts to advance the semiconductor industry into the future.

Guest Speakers

Long-Term National Competitiveness

Sarah Kemp, Vice President, International Government Affairs, Intel
Steve Pinkos, Senior Director, National Security Affairs, Intel
Allin Hedge, Director, Asia/Middle East/Africa, Intel

Defense, the Defense Industrial Base (DIB), and Supply Chains

Carl McCants, Senior Adviser to the Director, DARPA

DoD and Public-Private Partnerships in Semiconductors

Todd Younkin, CEO, Semiconductor Research Corporation (SRC)
Maryam Cope, VP, National Center for the Advancement of Semiconductor Technology (Natcast)
Paul Cohen, Sr. Manager for ESDA and R&D, SEMI
Patrick Wilson, VP, MediaTek

From Silicon to Quantum: Fundamental Considerations

Kerry Bernstein, Modern Technology Solutions

The DIB, Regulatory Policy, and Congress

Matt Hicks from Northrop Grumman
Nazak Nikakhtar, Wiley Rein LLP
Jacob Smith, Office of Senator John Cornyn

Fabs in Space

Ashley Pilipiszyn, CEO and founder of Bresxar

Chip Advocacy and National Security

Jennifer Meng, Director of Global Policy, Semiconductor Industry Association (SIA)
Aaron Woolf, Director of Global Policy for Economic Security, SIA

Travel

Indiana Field Study

Students and faculty conducted a two-day site visit to Purdue University's West Lafayette, Indiana campus, which houses one of the nation's premier semiconductor industry research institutions, to discuss innovation in semiconductor research and Indiana's efforts to build a semiconductor hub. A cluster for workforce development and innovation, the campus incorporates both academic and corporate advancements for semiconductor leadership. A key strength for Purdue's microelectronics program is its focused support for national security needs. The seminar met with a wide variety of Purdue organizations including the Birck Nanotechnology Center, the Purdue Policy Research Institute, and the Purdue Military Research Institute. The team also met with SK Hynix, MediaTek, and SkyWater Technology.

New York Field Study

Students and faculty visited IBM and GlobalFoundries in New York State. At IBM's Thomas J. Watson Research Center, participants discussed the company's advanced research into bleeding-edge semiconductors, AI, and quantum computing. At GlobalFoundries' Fab 8 in Malta, NY, the company presented an in-depth briefing on their role as a critical partner providing secure, legacy chips to the defense industry, described their vision for future opportunities and challenges, and led a fully clean-suited tour inside their pure-play semiconductor foundry.

Portland, Oregon

Another key cluster in Oregon, the "Silicon Forest", brought the team to conduct a week-long visit to the region's long-established semiconductor hub in the Portland metropolitan area. Students benefited from numerous engagements, including with AI futurist Steve Brown, the Provenance Chain Network, Intel, Lam Research, Hewlett-Packard, NuScale Power, Tektronix, Siltronic, Microchip, onsemi, Cadence, VintageTEK, Portal Space Systems, Anthropogenic Advanced Impact Intelligence, Business Oregon, and the City of Hillsboro. During these engagements, participants discussed the future of the U.S. semiconductor industry, technological advancements, as well as the DoD's requirements for both leading-edge and legacy chips.

Malaysia and Vietnam

To more fully understand the global nature of the industry, the seminar visited three cities in Southeast Asia: Penang, Malaysia; Ho Chi Minh City, Vietnam; and Hanoi, Vietnam. Malaysia and Vietnam are not only manufacturing hubs but budding innovation centers as well. The seminar met with U.S. companies, foreign firms, and U.S. Government leaders. Engagements included meetings with Intel, onsemi, Vitrox, Amkor, Arizona State University, Boston Consulting Group, Analog Devices, Motorola, Keysight Technologies, FPT Semiconductor, InvestPenang, the U.S. Consulate in Ho Chi Minh City, and the U.S. Embassy staff in Hanoi. Briefings and dialogue emphasized Malaysia and Vietnam's roles in the semiconductor supply chain, workforce development, and the future of advanced assembly, testing, and packaging.

EXECUTIVE SUMMARY

This paper analyzes the critical challenges facing the U.S. semiconductor industry and provides strategic recommendations to strengthen national competitiveness, national security, and technological leadership. It examines four key areas: securing critical inputs, addressing workforce shortages, advancing packaging technologies, and fortifying defense microelectronics. The paper highlights vulnerabilities in the supply chain, the urgent need for domestic talent development, and the importance of reshoring advanced semiconductor production. It also explores how AI-driven manufacturing, wargaming exercises, and policy interventions can mitigate risks and enhance resilience. The proposed solutions, including targeted investments, regulatory reforms, and international collaboration, aim to ensure the United States maintains its semiconductor leadership in the face of growing global competition, particularly with China.

INTRODUCTION

Strengthening U.S. semiconductor production capabilities is a clear and present challenge impacting national security, economic health, and global competitiveness. Intensifying Great Power Competition with China highlights the importance of this critical industry. Over the past several decades, much of the United States' semiconductor production has shifted overseas, ceding ground to allies and rivals alike. Additionally, the Department of Defense's (DoD) demand for semiconductors has dwindled to just a small portion of the market, with limited influence over industry-wide trends. Availability of semiconductors is a critical issue for the DoD and the nation. This paper explores four decisive challenges for strengthening U.S. capabilities, with recommendations on how to overcome key challenges.

The first section discusses critical production inputs, including materials and equipment, that represent imperatives for national security. The paper analyzes the industry using the SCP model (Structure, Conduct, Performance), acknowledges U.S. achievements, and summarizes DoD efforts to secure supply chains. It recommends five policy changes to ensure that the United States will regain its lead and secure the supply chain of semiconductors in the future.

The second section discusses labor challenges. A key finding is that the US needs a more coordinated national-level approach. The paper establishes five core objectives, for example, actions regarding basic education, higher education, training, and immigration, identifies the impact on national interests, and recommends five policies to ensure an adequate, skilled labor force.

The third section highlights the importance of assembly, testing, and packaging (ATP), which historically has not received as much attention in the United States as design or wafer production. The section summarizes a decades-long trend of offshoring and outsourcing before exploring how new packaging technologies are key to continuing advances in semiconductor performance. The paper recommends four policies to bring increasingly important advanced AT capacity back to the United States.

Finally, the fourth section addresses security of microelectronics. It emphasizes structural reforms for DoD and the nation regarding, emphasizing the shortcomings of the fragmented policies that exist today. The paper recommends creating a unified policy framework, strengthening enforcement, and improving integration with allies to ultimately deliver the security the United States needs.

The appendices address two additional issues with important implications for the semiconductor industry. Appendix A addresses the impact of the rapid growth and availability of generative artificial intelligence on the semiconductor industry. Appendix B explores how wargaming may address key challenges in semiconductor production.

ATOMS TO ADVANTAGE: SECURING THE MATERIALS AND TOOLS BEHIND AMERICA'S SEMICONDUCTOR EDGE

Framing the Issue

Semiconductors are the backbone of the United States' technological, economic, and national security advantage. However, critical material supply chain fragility and availability of precision tooling that powers chip production are strategic vulnerabilities that must be addressed.

Raw materials are the earliest inputs to the microchip value chain yet may be the most precarious to secure. China has exerted focused effort to control the value chain, making raw materials less widely available and more consequential. Rare earth elements (REEs), superabrasives, and ultra-high purity (UHP) wet chemicals – essential inputs for the 50 types of sophisticated tools for manufacturing next-generation semiconductors – remain overwhelmingly controlled by China.[1] In parallel, advanced lithography tooling exposes the United States to dependence on allied foreign suppliers, like the Netherlands' ASML, Which holds a monopoly on the crucial Extreme Ultraviolet (EUV) lithography technology.

This section argues that ensuring that a resilient supply chain for critical inputs is a national security imperative. It examines the risks posed by China's material control, assesses current policy gaps, and proposes a strategic framework for mitigating supply vulnerabilities. The solution requires a multipronged strategy that enhances domestic production, leverages international partnerships, and aggressively invests in next-generation sustainable technologies to ensure the United States maintains its competitive edge in semiconductor manufacturing.

Background

During the Cold War, the United States achieved microelectronic technological breakthroughs as the DoD and other agencies, like the National Aeronautics and Space Administration (NASA), revolutionized weaponry and strategic capabilities. However, in the 1970s, the United States began to cede its microelectronic fabrication superiority to Southeast Asia's large population of educated and inexpensive labor. Shortly thereafter, China discovered the world's largest deposit of REEs in its Bayan Obo mine in Mongolia, leading to a concerted effort to focus China's resources on space, information technology, laser technology, automation, and new materials. China created a holistic framework to dominate the critical materials value chain.[2]

At the same time, the United States abandoned its efforts to retain market share. From the 1960s to the 1980s, the United States led global production of rare earth oxides, metals, and alloys. Superabrasives, once a domain of U.S. leadership and essential for over 60% of

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[1] Antonio Varas, Raj Varadarajan, Ramiro Palma, Jimmy Goodrich, and Falan Yinug, "Strengthening the Global Semiconductor Supply Chain in an Uncertain Era," Boston Consulting Group, April 2021, https://www.bcg.com/publications/2021/strengthening-the-global-semiconductor-supply-chain.

[2] Joanne Abel Goldman. "The U.S. Rare Earth Industry: Its Growth and Decline." *Journal of Policy History: JPH* 26, no. 2 (04, 2014): 139–166. doi: https://doi.org/10.1017/S0898030614000013. https://login.nduezproxy.idm.oclc.org/login?url=https://www.proquest.com/scholarly-journals/u-s-rare-earth-industry-growth-decline/docview/1695738516/se-2.

semiconductor production steps, were forfeited in favor of comparative trading advantage. The United States introduced stringent environmental policies while labor costs increased. In the 1970s, two large chemical processing companies for REEs abruptly shut down due to an inability to meet to environmental policies.[3]

Analysis

Structure:

Concentration defines market structures across REEs, superabrasives, UHP chemicals, and lithography tooling. China maintains near-monopolistic control over the extraction and processing of REEs, industrial diamonds, and specialized chemical feedstocks. China's economic statecraft leverages currency devaluation, subsidizes overproduction, and manipulates prices to shut others out.[4] State-backed enterprises exacerbate the problem, accepting sustained losses to support national objectives.[5, 6]

Additionally, ASML holds a true monopoly on EUV lithography equipment. This structural concentration amplifies the vulnerability of downstream manufacturing and severely limits diversification options. With fewer than 60 units produced annually, each EUV machine is profoundly important. Any disruption to ASML or its critical suppliers would cause significant disruption to chip production.

Together, these chokepoints form a weak strategic flank for the United States. Without strengthening actions across multiple fronts - resource independence, technological innovation, and allied coordination – these economic and national security vulnerabilities represent unacceptable risk.

Conduct:

China's campaign to control critical materials is key to understanding the industry. In 2021, China consolidated its state-owned enterprises to create the China Rare Earth Group, Ltd, "a megafirm and largest of its kind in the world."[7] This consolidation resolved a fractured manufacturing base and consolidated state resources, allowing China to control the global supply

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[3] Ibid.

[4] Low cost anchors the entire Chinese industrial base. From the most upstream stages of any given industrial value chain, China conscientiously trades regulatory and environmental safety for cost advantage.

[5] Tellingly, the Chinese government's incremental capital to output ratio (ICOR) tripled from 3 to 9 between 2007 and 2018.
Steven Brent, PhD, ES-6134, Industrial Mobilization Competition, Academic Year 2024-2025, Lesson 22: Lecture, "PRC Innovation-Driven Development Strategy," to the National Defense University Eisenhower School for National Resource and Security Strategy Economics class, November 07, 2024.

[6] Individual companies "eat each other's lunch by competing on the slimmest margins" to attract these inefficient government subsidies.
Ibid.

[7] Qian Zhou and Sofia Brooke, "China Merges Three Rare Earths State-Owned Entities to Increase Pricing Power and Efficiency," *China Briefing*, January 12, 2022. https://www.china-briefing.com/news/china-merges-three-rare-earths-state-owned-entities-to-increase-pricing-power-and-efficiency/.

of 30-40% of global REE production and offer competitively low prices for raw and processed minerals.[8]

In 2010, China blocked REE mineral exports to Japan following a diplomatic dispute over the Senkaku Islands. During what became known as the Senkaku Crisis, neodymium and dysprosium prices spiked by almost 1,300%, crippling Japan's electronics and automotive sectors and sending shockwaves through global production.[9] [10] China's export controls on gallium and germanium leave the United States vulnerable to an adversarial competitor.[11]

The Dutch firm ASML charted a different path to its specialized EUV technology. ASML identified a technology gap and partnered with multiple microelectronics companies, like Intel, TSMC, and Samsung, to galvanize research and development funding. The EU and the Dutch governments provided additional funds and support. ASML succeeded, and despite the importance of the resulting technology, other firms have been unable to develop EUV production technology.

The key to these successes is a seamless, long-term strategy. In contrast, the United States fragments responsibilities across eight federal agencies and multiple international partnerships.[12] This fragmentation dilutes urgency, leads to bureaucratic duplication of effort, and undermines a coherent strategic approach.

Performance:

These structural and conduct patterns present systemic risk at multiple levels. Strategic material fault lines, exposure to foreign nations for essential components, and dependency on foreign-controlled technologies undermine the U.S. position. For example, China now controls 98% of the world's supply of gallium, 93% of germanium, and 97% of arsenic. UHP wet chemicals, critical to wafer cleaning, etching, and surface preparation, are likewise susceptible to Chinese control. Nearly 100% of global supply for key inputs, such as high-purity sulfuric acid

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[8] Kristin Vekasi, "Chinese Rare Earth Consolidation a Cause for Concern," East Asia Forum, March 30, 2022, https://eastasiaforum.org/2022/03/30/chinese-rare-earth-consolidation-a-cause-for-concern/.

[9] Ming Hwa Ting and John Seaman, "Rare Earths: Future Elements of Conflict in Asia?" Asian Studies Review 37, no. 2 (2013): 237.

[10] Bradley S. Van Gosen, Philip L. Verplanck, Keith R. Long, Joseph Gambogi, and Robert R. Seal II, The Rare-Earth Elements: Vital to Modern Technologies and Lifestyles, US Geological Survey Fact Sheet 2014–3078 (November 2014): 1.

[11] Alvin Camba, "A Federal Critical Mineral Processing Initiative: Securing U.S. Mineral Independence from China," War on the Rocks, April 14, 2025, https://warontherocks.com/2025/04/a-federal-critical-mineral-processing-initiative-securing-u-s-mineral-independence-from-china/.

[12] ChatGPT, response to "How many government agencies, executive orders, and acts are involved with critical minerals, and How many international partnerships and alliances is the US involved in for critical minerals?" April 19, 2025, OpenAI. See Annex 1 for additional information.

and isopropyl alcohol, emanates from Chinese producers.[13] [14] [15] While the Dutch have remained allies, ASML is the only producer of advanced EUV machines necessary for producing leading-edge chips. A disruption in ASML's production line, or a geopolitical shift causing the Dutch to become closer partners with China, could fundamentally shift the strategic advantage.

The United States' CHIPS Act has improved reshoring domestic chip fabrication, although it is still a nascent effort. The U.S. Geological Survey (USGS) reported that of the 50 critical minerals tracked by the Department of the Interior, the United States is 100% reliant on imports for 12 and more than 50% for another 28.[16] The United States needs a resilient, high-tech industrial economic foundation capable of effectively supporting a robust defense sector. A focused effort that channels the practicalities of the structure, conduct, and resultant performance of critical inputs must serve as the foundation of this effort.

Contemporary U.S. Achievements - Technological Innovations and Federal Action

Resilience in critical materials and lithography technology is not achievable through increasing resource extraction alone.

To address REEs, the United States underwrites the Critical Minerals Hub (CMH), funded by the Department of Energy (DOE). Under the CMH, DoE invested $17.5 million in 2024 to explore novel reclamation techniques such as coal ash extraction and component end-of-life recycling.[17] Other promising initiatives include artificial intelligence-driven mineral exploration, green chemistry, and bioleaching. These technologies could remove humans and toxic chemicals from the supply chain, potentially offsetting China's competitive advantages.[18] Still, the scale of these efforts are insufficient to assure industry needs will be met in the short term.

In superabrasives, the adoption of high-pressure, high-temperature (HPHT) and chemical vapor deposition (CVD) fabrication, combined with automation and nano-polycrystalline materials, promises the domestic production of performant synthetic diamonds and cubic boron

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[13] Shannon Davis, "U.S. Chip Expansions Squeezed by Shortages of Specialty Materials," Semiconductor Digest, August 8, 2022, https://www.semiconductor-digest.com/u-s-chip-expansions-squeezed-by-shortages-of-specialty-materials/.

[14] "Global Isopropyl Alcohol Market to Worth Over US$ 5.47 Billion By 2033," Astute Analytica, February 3, 2025, https://www.globenewswire.com/news-release/2025/02/03/3019293/0/en/Global-Isopropyl-Alcohol-Market-to-Worth-Over-US-5-47-Billion-By-2033-Astute-Analytica.html.

[15] Analysts forecast that the semiconductor industry demand for UHP wet chemicals will double by 2026. Ibid.

[16] Seth Amgott, "USGS: Value of U.S. Mineral Production Edged Up in 2024," U.S. Geological Survey, January 31, 2025, https://www.usgs.gov/news/national-news-release/usgs-value-us-mineral-production-edged-2024.

[17] "US DOE Announces $10M Funding for Critical Materials Innovation Hub," Ames National Laboratory (Department of Energy), November 21, 2024, https://www.ameslab.gov/news/us-doe-announces-10m-funding-for-critical-materials-innovation-hub.

[18] ChatGPT, response to "Can you provide a little more information on AI-powered exploration, autonomous mining, REE separation (Green Chemistry), and bioleaching? Can you please provide references?," April 17, 2025, OpenAI. See Annex 1 for additional information.

nitride (CBN) without the environmental barriers faced by mining.[19] These techniques reduce reliance on China and offer a cleaner, more adaptable alternative for precision semiconductor tooling.[20]

Lithography technologies are poised for transformation as well. China's pursuit of alternative lithography techniques, such as Nanoimprint Lithography (NIL) and Directed Self-Assembly (DSA), aims to bypass EUV restrictions.[21] Meanwhile, U.S. investments in multi-beam lithography, e-beam lithography, and photonic computing could enable leadership beyond the current EUV paradigm.[22]

Although diffuse, federal-level action is occurring for defense-specific purposes. The DoD awarded over $439 million to re-establish domestic REE supply chains, specifically $45 million to MP Materials.[23] MP Materials owns the United States' only vertically integrated rare earth mine and is expected to reach full capacity in 2025.[24] The DoD also provided funding to an Australian mining company to build a processing facility in Texas, allowing domestic mines to bypass China for these services.[25] The DoD and the DoE are also collaborating closely with American Rare Earths and a host of universities to explore novel REE separation processes.

DoD's efforts reflect an important shift to treat critical material and semiconductor tooling vulnerabilities as defense planning assumptions rather than economic externalities. If properly resourced and integrated, the DoD's role could serve as a model for broader national policy to rebalance structural dependencies, deter predatory conduct, and restore the performance profile necessary to sustain national security advantages.

Recommendations - Regaining the Strategic Advantage

Japan's Organization for Metals and Energy Security (JOGMEC) offers a compelling model for reform. By consolidating geological surveys, R&D investment, stockpiling, and financial assistance under a single agency, Japan reduced its REE import dependency from 90% to 58% in a decade.[26] Its reliance on China continues to decrease as partnerships with other

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[19] "Demystifying the Science Behind Superabrasives," Golden Gate Molders, February 21, 2024, https://www.goldengatemolders.com/post/demystifying-the-science-behind-superabrasives.

[20] HPHT, CVD, and nano-polycrystalline innovations help fabs overcome the costly tradeoff between precision and durability. HPHT and CVD not only enable domestic replication but also unlock manufacturing cost efficiencies that augur scalable growth. Additionally, the introduction of nano-polycrystalline structures offers next-generation performance gains for high-stress chip tooling applications.

[21] "Lithography: Paving the Way for Technological Advancement and Autonomy," Tech Insights, access May 14, 2025, https://www.techinsights.com/blog/ebook-lithography-gatekeeper-technological-independence-and-advancement.

[22] Multibeam Corporation, "Multibeam: Home," accessed May 14, 2025, https://multibeamcorp.com/.

[23] Glenn Zorpette, "The Coming Boom in Rare Earths," *IEEE Spectrum*, December 7, 2023, https://spectrum.ieee.org/rare-earth-elements-2666461932.

[24] Ibid.

[25] Ibid.

[26] Nayan Seth, "How to Diversify Mineral Supply Chains? A Japanese Agency Has Lessons for All," *New Security Beat*, August 15, 2024, https://www.newsecuritybeat.org/2024/08/how-to-diversify-mineral-supply-chains-a-japanese-agency-has-lessons-for-all/.

countries, like Australia, grow into beneficial REE trade relationships.[27] International efforts such as the Minerals Security Partnership (MSP) illustrate growing cooperation but remain advisory rather than operational.[28] Similarly, while EUV export controls coordinated among the United States, the Netherlands, and Japan have succeeded thus far, sustaining allied alignment requires continuous diplomatic investment.[29]

The pathway to fortifying the United States' microelectronics foundations requires a deliberate national strategy, sustained public-private investment, assertive defense-industrial integration, and coherent governance action. Building resilience at the upstream nodes of the semiconductor value chain demands also demands international coordination, technological innovation, and institutional reform. The following five mutually reinforcing policies will help secure critical materials and technologies.

Improve Domestic Production: The United States must prioritize full-spectrum domestic capacity for REEs, superabrasives, and UHP wet chemicals. Incentive structures—such as production tax credits, direct grants under the Defense Production Act Title III, and accelerated permitting timelines—should be explicitly tailored to upstream processing and material refinement. Lessons from MP Materials' vertically integrated model at Mountain Pass demonstrate the viability of U.S.-based extraction and downstream value capture when federal support bridges early capital barriers.[30] Similarly, fostering a domestic superabrasive sector through HPHT and CVD technology investments will be critical to restoring U.S. capabilities in precision wafer tooling.

The National Defense Stockpile: The DoD should reframe the National Defense Stockpile as an active instrument of economic statecraft. Current stockpile composition and authorization levels, still largely shaped by Cold War-era assumptions, are misaligned with Great Power Competition-era vulnerabilities. A modernized framework must explicitly include REEs, key superabrasives, and UHP wet chemical feedstocks essential to the defense microelectronics supply chain. Moreover, new mechanisms, such as offering tax incentives for private-sector contributions to stockpile inventories, would increase volume while alleviating federal budgetary constraints. The stockpile should evolve from a passive emergency reserve to a dynamic buffer actively managed for industrial readiness and surge capacity.

Allied Coordination and Friendshoring: While domestic reindustrialization is critical, global supply chains' economic and geological realities necessitate deepened collaboration with trusted allies. Programs such as the Minerals Security Partnership (MSP) and bilateral critical minerals agreements with Japan and Australia should be expanded into a true industrial alliance model. Joint investment vehicles, focused not only on mining but also on refining, recycling, and

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[27] Ibid.

[28] "Minerals Security Partnership," US Department of State, accessed April 17, 2025, https://www.state.gov/minerals-security-partnership.

[29] Sujai Shivukumar et al., "Balancing the Ledger: Export Controls on U.S. Chip Technology to China," Center for Strategic and International Studies (CSIS), February 21, 2024, https://www.csis.org/analysis/balancing-ledger-export-controls-us-chip-technology-china .

[30] "MP Materials Reports Third Quarter 2023 Results," MP Materials, November 2, 2023, https://investors.mpmaterials.com/investor-news/news-details/2023/MP-Materials-Reports-Third-Quarter-2023-Results/default.aspx.

alternative material development, can dilute China's control of upstream inputs without exposing single points of failure.[31] The DoD must further leverage its Foreign Military Financing (FMF) authorities, the National Technology and Industrial Base (NTIB) framework, and defense cooperation agreements to integrate allied material production capacity into U.S. contingency planning and acquisition strategies, ensuring that strategic minerals underpinning the defense industrial base remain secure even in contested environments.

Institutionalize Whole-of-Government Critical Materials Strategy: The fragmented agency landscape lacks the coordination necessary to achieve strategic scale and speed. To unify efforts, the United States should establish a National Critical Materials Coordination Office (NCMC) within the Executive Office of the President, reporting to both the National Economic Council and the National Security Council. This office would synchronize policy and funding across Defense, Energy, Commerce, and State Departments; oversee critical mineral R&D; monitor foreign investment; and liaise with allied industrial partners.

Reshoring domestic REE and superabrasive capacity will require $18 billion over ten years, while stockpiling efforts will need an additional $2-4 billion. An effective NCMC would streamline bureaucratic processes, deconflict interagency roles, and fast-track permitting and investment approvals. These efficiencies are essential to overcome the longstanding “red tape” barrier to industrial revitalization.[32] [33]

Additional investment will be needed to reduce reliance on foreign lithography. The DoE has already committed $179 million to the Extreme Lithography & Materials Innovation Center (ELMIC) at Lawrence Livermore National Laboratory.[34] However, this effort must be scaled to ensure future capability beyond EUV. Combined, these priorities bring expected federal costs above $22 billion.

The DoD should serve as a principal policy driver within the NCMC, ensuring alignment with defense industrial base requirements and force design needs. Like energy security post-1970s, critical materials security must be embedded into strategic planning as a foundational component of national power.

Issue Wrap-Up

The competition for microelectronics leadership is no longer simply economic - it is strategic. This study highlights that American technological and military primacy rests on fragile

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[31] "Minerals Security Partnership." U.S. Department of State, accessed April 17, 2025, https://www.state.gov/minerals-security-partnership.

[32] ChatGPT, response to “How much money would you estimate that the US federal government would have to subsidize to reshore domestic rare earth element and superabrasive industries to make them economically competitive?,” April 17, 2025, OpenAI. See Annex 1 for additional information.

[33] ChatGPT, response to “How much would it costs to store 2-5 years worth of critical minerals and superabrasives to support the US domestic microelectronics industry?,” April 17, 2025, OpenAI. See Annex 1 for additional information.

[34] “Department of Energy Announces $179 Million for Microelectronics Science Research Centers,” U.S. Department of Energy, December 23, 2024, https://www.energy.gov/science/articles/department-energy-announces-179-million-microelectronics-science-research-centers.

upstream foundations: rare earth elements, superabrasives, ultra-high-purity chemicals, and next-generation lithography. At each node, the United States faces structural vulnerabilities, predatory competitor behavior, and growing risks to its industrial and defense base. China's deliberate consolidation of material supply chains and its weaponization of market access expose critical fault lines. Meanwhile, U.S. dependence on a concentrated allied supply chain for EUV lithography introduces distinct systemic risks.

Material inputs are a key ingredient for a thriving semiconductor industry, and an adequate labor force is required to deliver products to an expanding market.

BUILDING THE MICROELECTRONICS WORKFORCE FOR THE FUTURE

Framing the Issue

Semiconductors underpin nearly every aspect of modern American society, enabling advancements in national defense, artificial intelligence (AI), telecommunications, healthcare, and renewable energy. However, over the past several decades, the United States' microelectronics production capacity and skilled labor base have steadily declined. In 1990, the United States produced 37% of the world's semiconductors; today, that number has fallen to just 12%.[35] This contraction in domestic manufacturing propagated a severe talent shortfall—an estimated 67,000 skilled positions are expected to go unfilled by 2030.[36] The United States invests heavily in domestic semiconductor manufacturing; however, the supporting workforce infrastructure remains inadequate, fragmented, and uncoordinated. The Semiconductor Industry Association projects a shortfall of 67,000 technical workers in the semiconductor industry by 2030, with broader STEM workforce gaps nearing 1.4 million.[37] This labor shortage is concentrated in technician and engineering roles, especially in fabrication and advanced packaging—two areas where the United States must re-shore capabilities to counter rising Chinese dominance.

Workforce development remains fundamental to building a more sustainable, resilient semiconductor industry. Despite the CHIPS and Science Act's $52.7 billion in allocated funding, only $2.7 billion (about $8.30 per person in the US) is dedicated to workforce development. Existing programs like the Good Jobs Challenge and Tech Hubs also seek to strengthen the workforce, but national-level coordination remains lacking. Most training programs are designed to meet local corporate needs rather than strategic national objectives, with little standardization to enable workforce mobility. Furthermore, only 3% of U.S. engineering graduates enter the semiconductor sector, and the absence of standard industry-recognized credentials makes skill transferability difficult across regions and firms.[38]

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[35] Semiconductor Industry Association, *Chipping Away: Assessing and Addressing the Labor Market Gap Facing the U.S. Semiconductor Industry* (Washington, D.C.: SIA, 2023), https://www.semiconductors.org/chipping-away-assessing-and-addressing-the-labor-market-gap-facing-the-u-s-semiconductor-industry/.

[36] Ibid

[37] Bill Wiseman et al., *Reimagining Labor to Close the Expanding US Semiconductor Talent Gap.* McKinsey & Company, August 2024, https://www.mckinsey.com/industries/semiconductors/our-insights/reimagining-labor-to-close-the-expanding-us-semiconductor-talent-gap.

[38] Ibid.

The dilemma also extends to policy bottlenecks. Immigration caps and backlogs make retaining international students graduating from top U.S. institutions difficult. For example, international graduates from India and China—representing over 60% of semiconductor-focused PhDs in the United States—can wait decades for permanent residency.[39] Meanwhile, China has aggressively implemented workforce development and industrial policies under the "Made in China 2025" and "National IC Plan," investing over $150 billion and producing over 600,000 engineers annually.[40]

To address this growing set of challenges, the United States must develop a coordinated national-level approach to create and sustain a resilient microelectronics workforce. This section assesses the strategic objectives of national efforts to rebuild semiconductor talent, analyzes the policy and structural barriers slowing workforce expansion, and explores the institutional strengths and policy levers necessary to succeed. It recommends specific policies to accelerate and scale solutions as a blueprint for positioning the United States for a strengthened role in the global semiconductor industry.

Analysis – Interests, Objectives, and Existing Programs

Interests

The urgency of developing a robust domestic semiconductor workforce transcends economic concerns—it is a foundational issue of national security and long-term global competitiveness. The following considerations make strengthening the microelectronics workforce an important national interest.

National Security: Semiconductors are integral to all major defense platforms, including precision-guided munitions; intelligence, surveillance, and reconnaissance (ISR) systems; space-based assets; and cyberspace infrastructures. The dependence on foreign semiconductor labor and manufacturing—particularly from Taiwan and China—introduces systemic vulnerabilities ripe for exploitation in conflict. Notably, China's military strategy of "systems destruction warfare" explicitly seeks to undermine adversaries' technological infrastructures as a first-strike tactic.[41] Relying so heavily on critical technology production within China and its immediate vicinity is a profound national security vulnerability.

Economic Competitiveness: Workforce limitations are already impeding the scalability of U.S. fabrication and packaging capacity. Without ample skilled labor, firms may be forced to defer or relocate planned investments abroad despite federal incentives such as the CHIPS Act. Failure to produce the required workforce will result in missed economic opportunities and the

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[39] Semiconductor Industry Association. *Semiconductor Workforce Development: A Policy Blueprint (*Washington, D.C.: SIA, 2024), https://www.semiconductors.org/workforceblueprint/.

[40] Arrian Ebrahimi, "China Boosts Semiconductor Subsidies as US Tightens Restrictions," *The Diplomat*, September 28, 2023, https://thediplomat.com/2023/09/china-boosts-semiconductor-subsidies-as-us-tightens-restrictions/.

[41] Jeffrey G. Engstrom, *Systems Confrontation and System Destruction Warfare: How the Chinese People's Liberation Army Seeks to Wage Modern Warfare*, Research Report, RR-1708-OSD (Santa Monica, CA: RAND Corporation, 2018), https://www.rand.org/pubs/research_reports/RR1708.html.

erosion of high-value jobs across sectors such as automation, artificial intelligence, photonics, and advanced manufacturing.

Technological Leadership: The next generation of global breakthroughs—whether in AI, 6G telecommunications, or quantum computing—relies on the timely availability of advanced microelectronics. A lack of scientists, engineers, and technicians trained in semiconductor-relevant domains jeopardizes the United States' ability to drive innovation and set international technology standards.

Supply Chain Resilience: Increasing domestic capacity without parallel investments in workforce development will result in under-utilized fabrication facilities, idle capital, and unfilled manufacturing jobs. The United States currently produces 12% of global semiconductors and controls less than 5% advanced packaging capacity.[42] Without workforce expansion, attempts to bolster physical infrastructure will fail to deliver strategic outcomes.

Meanwhile, China is executing decades-long, state-coordinated strategies to cultivate semiconductor expertise through education reform, funding incentives, and global recruitment. In contrast, the United States has remained reactive. Unless a proactive, nationally unified workforce strategy is implemented, the United States risks a decline in its technological sovereignty and ability to respond to future security and economic challenges.

Objectives

To address the workforce challenges in the semiconductor industry, an integrated strategy must mobilize educational institutions, industry stakeholders, and government agencies. Five core objectives define this strategic imperative:

Developing a Scalable and Sustainable Talent Pipeline: A long-term supply of skilled workers—spanning technicians, engineers, and data scientists—is essential to meet the demand for talent in fabrication, advanced packaging, and semiconductor research and development. This requires strategic investment across the entire talent lifecycle, from early STEM engagement to graduate-level specialization.

Expanding Semiconductor-Focused STEM Education: Updating and aligning K–12, community college, and university curricula with the needs of the semiconductor sector is foundational. This includes integrating lab-based learning, cleanroom exposure, and digital systems design into academic programs. Institutions such as Purdue University have already successfully offered tailored semiconductor degrees and collaborate with local institutions to create pipelines of talent.[43]

Institutionalizing Apprenticeships and Credentialing Programs: National certification frameworks and registered apprenticeships, modeled on programs like Semiconductor Career and Apprenticeship Network (SCAN) and Growing Apprenticeships in Nanotechnology and

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[42] Semiconductor Industry Association. *2024 State of the U.S. Semiconductor Industry* (Washington, D.C.: SIA, 2024).

[43] Semiconductor Industry Association. *Semiconductor Workforce Development*.

Semiconductor (GAINS), must bridge academic theory with industrial practice.[44] These pathways ensure workers are industry-ready, not just job-ready, and can transition across geographies and employers.

<u>Strengthening Public-Private-Academic Partnerships (PPAPs):</u> Programs such as Scalable Asymmetric Lifecycle Engagement (SCALE) offer a blueprint for aligning academic training with Department of Defense (DoD) and private sector requirements. A robust national workforce strategy must expand and institutionalize such models, linking them to regional innovation ecosystems and federally funded research centers.

<u>Modernizing Immigration and Retention Policies:</u> While U.S. workers are preferred, immigration will remain a significant source of talent to supplement the domestic workforce. Immigration reform is critical to maintaining U.S. competitiveness. Current bottlenecks in the H-1B visa process and green card allocations restrict the ability of U.S.-educated international students to remain and contribute to the workforce. A streamlined and prioritized system for STEM graduates is essential to sustain innovation capacity.

Regional workforce centers and virtual training platforms should bridge urban innovation hubs with rural and underserved communities. Federal programs, such as the Defense Civilian Training Corps, traditionally geared toward public sector service, should be expanded to support private sector pathways in semiconductor research and manufacturing. Such integration ensures the national approach is comprehensive and adaptive to regional workforce needs.

Existing Programs

The success of a workforce strategy depends not only on clear goals but also on the ability to integrate and scale proven institutional frameworks. The United States is not starting from scratch. A range of programs, capabilities, and innovation ecosystems, if better coordinated, can serve as powerful levers for transformation.

First, the 2022 CHIPS and Science Act created crucial infrastructure by establishing the National Semiconductor Technology Center (NSTC) and its affiliated Workforce Center of Excellence (WCoE). These platforms are designed to standardize curriculum development, consolidate internship and apprenticeship networks, and serve as a central hub for national labor market data and skills forecasting. With appropriate resources and governance, the NSTC and WCoE can become foundational to long-term workforce resilience.

Second, the SCALE initiative, spearheaded by Purdue University, exemplifies a high-functioning public-private-academic partnership. SCALE links DoD microelectronics needs to university programs and incorporates hands-on technical training, security clearance preparation, and real-world problem-solving exercises. This model is replicable and requires funding and support to deploy across other regional academic hubs.

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[44] "Growing Apprenticeships in Nanotechnology and Semiconductors (GAINS)," National Institute for Industry and Career Advancement (NIICA), accessed April 18, 2025, https://www.niica.org/gains/.

Third, industry-led apprenticeships like SCAN and GAINS demonstrate how federal investment can be leveraged to produce immediate workforce outcomes. These programs align with registered apprenticeship frameworks and provide accelerated, applied training to entry-level fabrication, design, and packaging workers. Additionally, the United States benefits from a geographically dispersed but technically dense network of innovation clusters—including Silicon Valley, Austin, Albany, Portland, and Phoenix—where leading firms such as Intel, GlobalFoundries, TSMC, and Samsung maintain operations that are central to microelectronics ecosystems in their regions. These ecosystems co-locate industry, academia, and national labs, offering ideal conditions for workforce scaling through collaborative research and localized talent development.

Finally, global comparisons offer further validation. The European Union's Chips Act and China's National IC Plan prioritize long-term education, training, and workforce infrastructure investments. These strategies have already led to significant gains in talent production and manufacturing capacity abroad. The United States, with its innovation leadership, institutional credibility, and financial resources, is well-positioned to mount a similar—if not superior—effort. These institutional assets provide a compelling foundation for a unified and enduring national microelectronics workforce strategy.

Recommendations

Developing a resilient, nationally coordinated workforce requires significant investments relative to the broader scale of semiconductor sector growth. A proposed investment with an estimated total of $15-25 billion over a ten-year period, strategically allocated across five key areas:

K-12 and Early STEM Pipeline Development ($4-6 billion)[45]: Funding must support curriculum modernization, competitive robotics programs (e.g., FIRST Robotics), educator training, and expanded STEM outreach to rural and underserved communities. These investments would lay the foundation for long-term interest, understanding, and proficiency in semiconductor-relevant disciplines for a wide range of young Americans.

Postsecondary Program Expansion ($5-7 billion)[46]: This category includes federal grants for modernizing community college and university training programs, building cleanroom laboratories, acquiring semiconductor processing equipment, and training specialized faculty to deliver advanced technical content.

National Credentialing and Apprenticeship Infrastructure ($2-3 billion)[47]: Establishing a federally recognized certification system and incentivizing employers to adopt registered apprenticeships will align competencies and improve talent mobility across regions.

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[45] Estimated cost to support 10,000 public schools, fund robotics programs and competitions, and provide STEM fellowships for 5,000 teachers.

[46] Estimated cost to fund 500 community colleges, 200 universities, scholarships for 50,000 students, and $1B of cleanroom lab construction.

[47] Estimated cost to develop national system, support 100,000 apprenticeships, and establish certification program.

Immigration Processing Modernization ($500 million)[48]: Though relatively modest, investments in streamlining visa processing and green card adjudication are critical to ensure the timely retention of international STEM graduates trained in U.S. institutions.

Regional Workforce Centers of Excellence ($4-6 billion)[49]: Funding is required to develop and sustain workforce centers co-located with the 31 federally designated Tech Hubs. These centers will coordinate regional curricula, align training with emerging research needs, and serve as talent incubators in partnership with NSF, DARPA, and industry.

When viewed in the context of the $450 billion in private-sector semiconductor manufacturing investments announced since the passage of the CHIPS Act, the proposed public investment in workforce development represents a comparatively small but strategically important commitment. Without it, capital investment will outpace the availability of skilled labor, limiting the impact of new facilities and expanded capacity.

Timeline

The construction of a resilient national semiconductor workforce cannot be achieved overnight, but requires sustained, phased investment over short-, medium-, and long-term time horizons. Each phase contributes critical components to a coherent talent development architecture:

Short-Term (1-3 Years): Initial efforts must focus on rapidly expanding technician training programs and launching a standardized national certification framework. These steps will enable a consistent baseline of industry-recognized competencies and provide immediate talent for fabrication and packaging facilities. Concurrently, the United States should expand existing models, such as SCALE and SCAN, to more regions. The United States should also intensify early STEM outreach—particularly in K-12 education— to build awareness of semiconductor careers. Immigration policy reforms, including extending Optional Practical Training (OPT) to five years and exempting of STEM graduates from H-1B caps, could be implemented swiftly to retain skilled foreign talent.

Medium-Term (4-7 Years): In this phase, the federal government should establish and operationalize workforce development centers across each of the 31 designated Tech Hubs. These centers would serve as regional anchors, coordinating dual-credit high school programs, standardizing semiconductor-relevant and other technical curricula, and integrating community colleges into advanced technical education. Support to institutions in the form of cleanroom laboratories and chip design facilities, ensuring students graduate with practical competencies while increasing the demand for domestic semiconductor tools.

Long-Term (8-15 Years): By the end of this horizon, the United States should achieve a steady-state semiconductor workforce pipeline. This would include a seamless progression from

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[48] Estimated cost to upgrade U.S. Citizenship and Immigration Services systems, hire and train 1,000 staff, and implement public-private partnership pilot.

[49] Estimated cost to establish 12 regional hubs, including facilities, faculty, training programs, and employer partnerships.

early education through postsecondary institutions, sustained lifelong learning programs, and efficient systems for international talent retention. In this model, industry, government, and academia would operate in a state of institutional coordination, consistently producing the workforce necessary to meet commercial growth and national defense requirements.

Issue Wrap-Up

The semiconductor workforce shortfalls present one of the most consequential challenges for the industry in the coming decade. The convergence of technological dependence, global competition, and domestic labor shortages has created a strategic inflection point, demanding comprehensive action.

With the necessary policies and resources to address critical inputs and the workforce, the United States must also address specific semiconductor technologies that will have the greatest impact in the near term.

ADVANCED PACKAGING: THE NEXT FRONTIER FOR MICROELECTRONICS

Framing the Issue

In order for the U.S. military to maintain the technological advantage over its adversaries, the Defense Industrial Base (DIB) must invest in the most impactful technologies that will shape the microelectronics industry. Advances in photonics, quantum computing, and organic-based computing have the potential to open important new aspects of microelectronics. However, advanced assembly, test, and packaging (ATP) will have the greatest impact in the near-term. This section will discuss ATP and the advances occurring in three-dimensional (3-D) design and build. It will then discuss the nascent but potentially disruptive technologies of photonics, quantum computing, and organic-based computing. The section concludes with recommendations for the United States to reshore advanced ATP and capitalize on disruptive technologies to provide the U.S. military with a continued advantage in warfare.

ATP is the segment of the semiconductor value chain that is responsible for integrating individual microchips onto a circuit board, performing functionality checks, and packaging the device for system-level integration. Although important, it has traditionally been considered a "low-value" segment of the value chain, prime for offshoring to locations with low labor costs, a less stringent regulatory environment, and favorable tax policies. [50] In 2021, the United States accounted for only 5% of global ATP capacity.[51] Specialized Outsourced Semiconductor Assembly and Testing (OSAT) companies emerged to accomplish the increasingly offshored ATP work.

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[50] Katie Canales, "Chips Are Difficult to Produce, and It's Cheaper for US Companies to Outsource," *Business Insider*, April 17, 2021, https://www.businessinsider.com/why-us-doesnt-make-chips-semiconductor-shortage-2021-4.

[51] Alice B. Grossman et al., *Semiconductors and the Semiconductor Industry*, CRS Report No. R45708 (Washington D.C.: Congressional Research Service, 2023), "Semiconductors and the Semiconductor Industry" (Congressional Research Service, April 19, 2023), 16, https://www.congress.gov/crs_external_products/R/PDF/R47508/R47508.5.pdf.

OSAT companies have evolved to integrate decreasing node size chips onto circuit boards. However, as microelectronics firms progressively shrank circuit elements to approach the physical dimensions of atoms, further miniaturization of node size becomes far more difficult. A fundamental shift in microprocessor design and ATP is needed to achieve further improvements in semiconductor performance. State-of-the-art innovations are now exploring three-dimensional design and stacking of microprocessor components to deliver these gains. ATP has the potential to shift from being an afterthought ripe for outsourcing to a central part of technological advantage.

Analysis

Advances in microelectronics have enabled the United States to fuse information across all domains and act on that information with precision at scale and speed. The driving technologies are advanced semiconductors that enable inexpensive sensors, AI, quantum computing, robotics, and precision long-range weapons.[52] The fusion of pervasive sensors paired with mass analytics enabled by advanced computing has revolutionized real-time detection and information processing.[53] The immense knowledge gained from these semiconductor technologies, coupled with precision kinetic and non-kinetic weapons, has enabled the theory of systems destruction warfare. This theory posits that wars are won through the ability ti disrupt, paralyze, or destroy an enemy's operational system.[54] The United States and China have recognized this revolution and have embraced system destruction warfare as the current method of modern warfighting.[55] Access to advanced semiconductors is essential to both China and the U.S. military capabilities and their strategy for waging war. Moreover, the nation that better develops and utilizes 3-D chips may achieve a technological advantage in war. The DIB recognizes this technology's significance for increasing weapon system performance and potentially reducing costs through reductions in size, weight, and power.

Advanced ATP is a Significant Evolutionary Capability

As the industry approaches the physical limitation of Moore's Law for integrated circuit size, a new dimension for improvement must arise. Veteran OSAT companies are investing in the research and development (R&D) necessary to push performance forward. They seek to expand market share in additional sectors, including defense, but focus primarily on commercial automotive and high-performance computing, including artificial intelligence. The following companies are currently the top five worldwide OSATs by market share:

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[52] Joint Chiefs of Staff, *Doctrine for the Armed Forces of the United States*, JP 1 (Washington, D.C.: Joint Chiefs of Staff, 2023), VI–1, chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/https://keystone.ndu.edu/Portals/86/Joint%20Warfighting.pdf.

[53] Joint Chiefs of Staff, *Doctrine*, VI–2.

[54] Engstrom, *Systems Confrontation,* iii.

[55] Ibid.

Rank	Company Name	Headquarters	Estimated Market Share (2024–2025)	Key Strengths
1	ASE Technology Holding Co., Ltd.	Kaohsiung, Taiwan	~30%	Scale, innovation, advanced packaging
2	Amkor Technology, Inc.	Tempe, Arizona, USA	~14%	Advanced packaging, global reach
3	JCET Group Co., Ltd. (Jiangsu Changjiang Electronics Technology)	Shanghai, China	~12%	R&D, domestic and global expansion
4	Powertech Technology Inc. (PTI)	Hsinchu, Taiwan	~8%	Memory packaging expertise
5	Tongfu Microelectronics Co., Ltd.	Suzhou, China	~5%	Cost efficiency, strong domestic presence

Table 1: Top 5 OSATs Worldwide[56]

Of these companies, only one is a U.S. firm. As this industry segment begins to drive performance gains in semiconductors and move up the value chain, foundries and other front-end semiconductor companies may pursue expanded roles in advanced ATP.

The following sections explore each of the three components of ATP and the importance to the reliable production of increasingly complex chips.

Assembly

Assembly requires multiple steps, and throughout those steps, testing is ongoing to ensure the die is connected and encapsulated correctly for the application it's designed for. The complexity of assembly is increasing with the demand to design and build in 3 dimensions. Companies are dealing with a product mix explosion driven by different global market sectors, whether automotive, artificial intelligence, or high-performance computing. The assembly process follows wafer preparation, die preparation, interconnection, and encapsulation. As the die is tested, connected, and encapsulated, several other steps in between and during these processes are driven by the end state application of the die. As more semiconductors become integrated into systems requiring high reliability levels, the assembly and packaging process must be near-zero defect. These processes take several weeks to complete final products and several months to scale for volume.

Testing

Testing is essential in all semiconductor fabrication as it ensures proper functionality and determines one of the most critical values in the ATP process: the yield of the fabrication process. The yield per wafer is where economies of scale during production are achieved. Additionally, testing is extremely critical to technologies that require high reliability, such as automotive, artificial intelligence, and space-tailored semiconductors.

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[56] Adapted from Kumar Priyadesh, "Top 10 OSAT (Outsourced Semiconductor Assembly and Test) Companies in 2024," *Semiconductor News*, August 26, 2024, https://techovedas.com/top-10-osat-outsourced-semiconductor-assembly-and-test-companies-in-2024/.

Testing consists of two larger categories, starting with wafer testing and finishing with package testing. Testing requires advanced tools that include microscopic probes to assess electrical, environmental/reliability, and structural defect analysis. Individual chips may undergo over 20 tests throughout the stages of production.

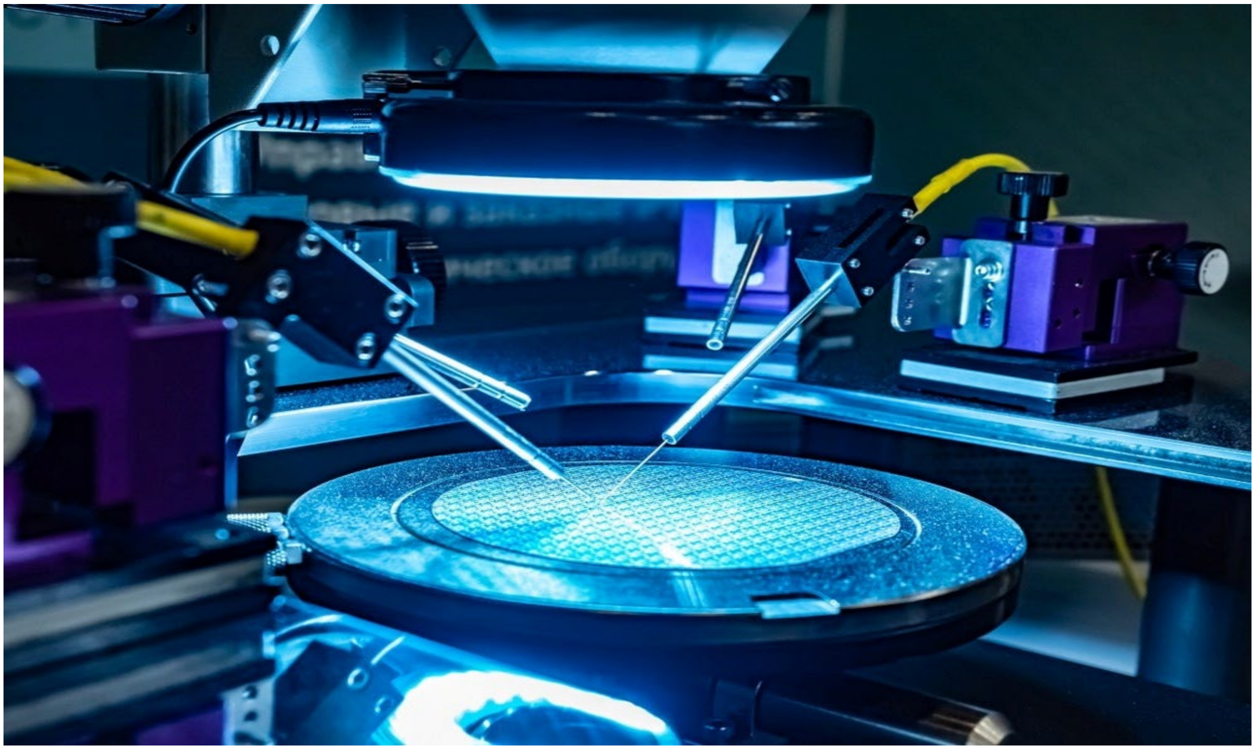

Figure 1: Wafer Testing with Probes[57]

Packaging

While assembly and test activities remain important to semiconductor production, rises in value and growth increasingly occur due to breakthroughs in packaging advances like three-dimensional design and integration (3-D). The classical approach to packaging has been in two dimensions (2-D), which has experienced incremental improvements for the last 40 years. Many common 2-D architectures were designed in the 1990s, starting with Multi-Chip Modules (MCMs), which resulted in multiple dies being integrated onto a common substrate. These techniques have always been confined to 2-D architectures. The jump to 3-D heterogeneous integration (3DHI) was first bridged by 2.5-D advances, which use an interposer, an electrical interface for increasing connection density for side-by-side die placement. 3-D ICs have a higher degree of integration with vertical stacking, promising dramatic ongoing increases in performance and reduced power consumption. However, 3DHI has numerous mechanical and thermal design challenges that require significant research and development.

Table 2 below charts the different technology categories and how new processes have evolved.

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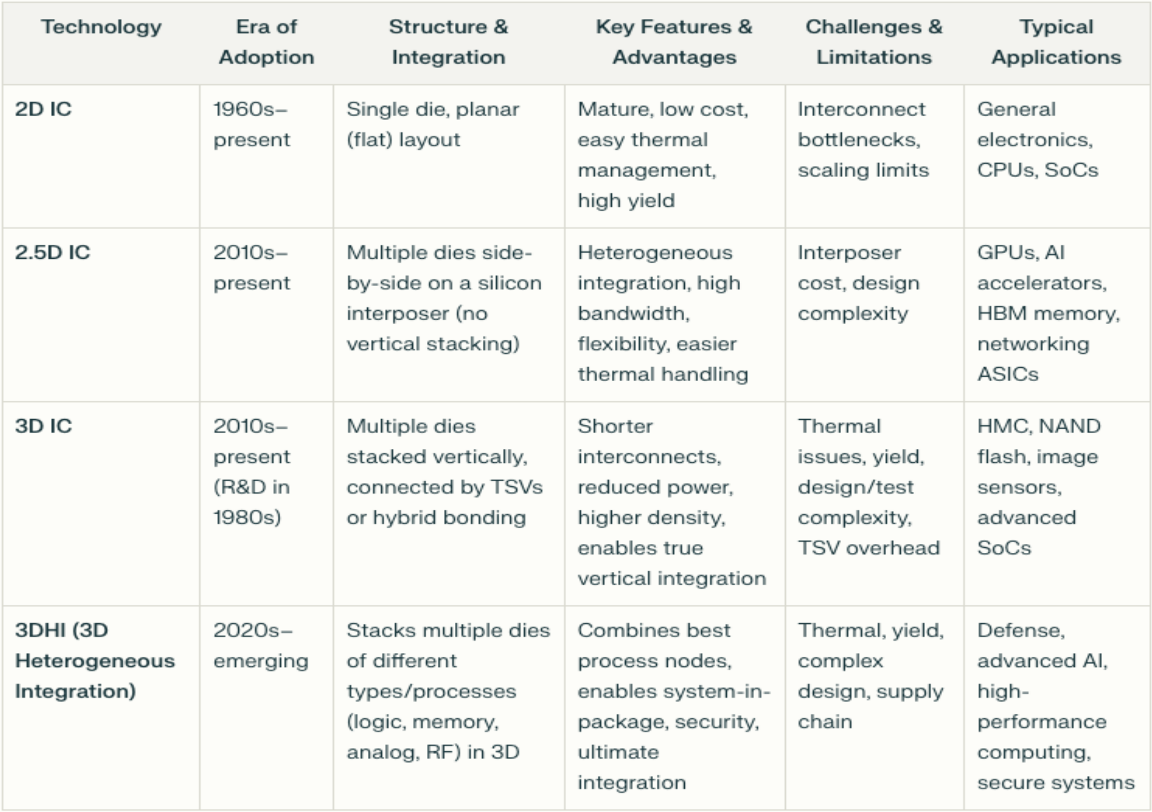
[57] Source: Ibtisam Abbasi, “A Closer Look at Semiconductor Test Equipment,” AZO Materials, August 30, 2022, https://www.azom.com/article.aspx?ArticleID=21992.



Technology	Era of Adoption	Structure & Integration	Key Features & Advantages	Challenges & Limitations	Typical Applications
2D IC	1960s–present	Single die, planar (flat) layout	Mature, low cost, easy thermal management, high yield	Interconnect bottlenecks, scaling limits	General electronics, CPUs, SoCs
2.5D IC	2010s–present	Multiple dies side-by-side on a silicon interposer (no vertical stacking)	Heterogeneous integration, high bandwidth, flexibility, easier thermal handling	Interposer cost, design complexity	GPUs, AI accelerators, HBM memory, networking ASICs
3D IC	2010s–present (R&D in 1980s)	Multiple dies stacked vertically, connected by TSVs or hybrid bonding	Shorter interconnects, reduced power, higher density, enables true vertical integration	Thermal issues, yield, design/test complexity, TSV overhead	HMC, NAND flash, image sensors, advanced SoCs
3DHI (3D Heterogeneous Integration)	2020s–emerging	Stacks multiple dies of different types/processes (logic, memory, analog, RF) in 3D	Combines best process nodes, enables system-in-package, security, ultimate integration	Thermal, yield, complex design, supply chain	Defense, advanced AI, high-performance computing, secure systems

Table 2: Packaging Overview[58]

An R&D investment in 3DHI promises the most significant capability and performance gains for the foreseeable future to meet the DoD's semiconductor needs. The DoD’s interest is evident in the CHIPS Act, where the National Advanced Packaging Manufacturing Program awarded over $1.4 billion to industry and academia to investigate the usability and scalability of 3DHI chips.

Additionally, DARPA has applied its culture and network since 2018 to focus on the Electronics Resurgence Initiative (ERI) 2.0, which focuses on reinventing domestic microelectronics manufacturing to ensure the United States can maintain its technological competitive advantage. DARPA has helped focus the industry and the national security sector on 3DHI and electronics development in extreme environments.[59] As an example, DARPA has worked with industry and academia on its Next Generation Microelectronics Manufacturing (NGMM) summit to help solve the technical challenges of 3DHI. NGMM includes three phases:

1) Phase 0 (complete): Performer teams worked to define, analyze, and make expert recommendations for representative 3DHI systems.

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[58] Max Maxfield, “2D vs. 2.5D vs. 3D ICs 101,” *EE Times*, April 8, 2012, https://www.eetimes.com/2d-vs-2-5d-vs-3d-ics-101/.

[59] “ERI Summit | What Is ERI?,” DARPA, accessed April 20, 2025, https://eri-summit.darpa.mil/what-is-eri.

2) Phase 1 (began September 2024): Establish the center's infrastructure and basic capabilities

3) Phase 2: Build 3DHI prototypes and automate essential processes to drive long-term success.[60]

Advanced packaging manufacturers must also innovate to realize the potential of 3DHI capabilities. Advances could open the pathway to disruption in the semiconductor ecosystem. The DoD recognizes this and has invested $49 million under the Re-shore Ecosystem for Secure Heterogeneous Advanced Packaged Electronics (RESHAPE) program. The contracts focus on low-volume, high-mix, secure 2.5-D and 3-D packaging production.[61] This is only a small investment focused on defense suppliers, but signals that DoD recognizes the importance of advanced packaging for national security applications.

Recommendations

The U.S. government should enact industrial policy to reshore ATP seeking to meet greater than 30% of the world's capacity, with a heavy focus on advanced ATP. This would provide a sufficient capability to develop microchips domestically, providing economic and military resiliency. To achieve this, the United States should implement four policies.

First, the U.S. government must provide grants to companies to build advanced ATP facilities. The semiconductor industry is in the midst of a highly disruptive and capital intensive process of expanding production across a number of steps. Grants would represent a meaningful injection of capital to strengthen industry's appetite to invest in domestic advanced ATP facilities amidst other industry investment.

Second, the United States must provide significant tax and utility breaks to aid the development of advanced ATP facilities. Pairing up-front grants with ongoing tax and utility breaks would offset the aggressive policies used by other nations to attract ATP facilities.

Third, the United States must require defense primes to implement a phased modernization program over 4 years to use advanced packaging technologies to integrate and optimize semiconductor components to reduce reliance on legacy and obsolete ICs.

Finally, the United States must introduce tariffs focused on offsetting the lower labor costs and unequal labor practices offshore. This would require specific messaging to draw a distinction between broader tariffs addressing trade imbalances but is important to maintain a level playing field for business decisions about reshoring.

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[60] "NGMM: Next-Generation Microelectronics Manufacturing," DARPA, accessed April 20, 2025, https://www.darpa.mil/research/programs/next-generation-microelectronics.

[61] John Hill, "US DoD Invests $49m in Local Advanced Semiconductor Packaging," *Army Technology*, January 25, 2024, https://www.army-technology.com/news/us-dod-invests-49m-in-local-advanced-semiconductor-packaging/.

Issue Wrap-Up

These policy recommendations form a strong basis for breaking the decades-long trend of offshoring and outsourcing ATP. They constitute a significant investment and may impact consumer prices, but recapturing competency and market share in this increasingly important stage of microelectronics production is important enough to justify these costs. Yet, even if the United States is successful, it is also crucial to address the security of U.S. semiconductors for national security needs.

SECURE DEFENSE MICROELECTRONICS: STREAMLINING DOD'S STRATEGY THROUGH GOVERNANCE AND POLICY ALIGNMENT

Framing the Issue

The technological superiority of the United States in defense systems is fundamentally dependent on secure and reliable access to advanced microelectronics. Semiconductors enable critical military capabilities, from precision-guided munitions to resilient communications. However, the Department of Defense (DoD) faces persistent challenges in safeguarding its supply chain amid intensifying global competition and emerging security threats. Although several programs have been established to mitigate these risks, their effectiveness is limited by fragmented governance, legacy system dependencies, and bureaucratic inefficiencies. Key policy drivers, including the CHIPS Act and Department of Defense Instruction (DoDI) 5200.44, provide a legal but fragmented framework for domestic semiconductor manufacturing revitalization. Only by consolidating oversight, enforcing consistent security standards, and integrating dual-use technological innovation can the United States modernize and fortify its microelectronics supply chain to sustain national security superiority.

Current DoD Approach: Programs and Policy Foundations

The DoD microelectronics acquisition approach relies on a complex ecosystem of programs and policies designed to secure critical semiconductor components for defense applications. While various programs individually focus on different aspects of the supply chain, from accreditation of domestic vendors to leveraging commercial innovation, they collectively aim to address the growing challenges of securing advanced microelectronics. These interconnected programs and policies form the DoD's multi-faceted approach to ensuring access to secure, reliable semiconductors in an increasingly complex global landscape.

Trusted Supplier Program (TSP): Securing Legacy and Trusted Components

Established in 2004 following Deputy Secretary of Defense Paul Wolfowitz's 2003 proposal, the Trusted Supplier Program (TSP) accredits domestic suppliers to produce defense-grade semiconductors under stringent security protocols.[62] Initially operated as the "Trusted Foundry Program" under National Security Agency (NSA) supervision through the Trusted Access Program Office (TAPO), the program began with IBM as the sole supplier before

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[62] Catherine Ortiz, "DoD Trusted Foundry Program: Ensuring 'Trust' for National Security and Defense Systems," NAVAIR DMSMS Branch, January 9, 2013, 8, https://jteg.ncms.org/wp content/files/documents/DoD%20Trusted%20Foundry%20Program_9Jan2013.pdf.

transitioning to Global Foundries in 2015. Today, the program includes 82 accredited facilities across the microelectronics lifecycle. However, it covers only 2 percent of the chips the DoD procures, primarily because its sole at-scale supplier, GlobalFoundries, can only produce chips at the 12 nm node and above, far behind industry leaders currently advancing technologies below 2 nm.[63, 64, 65] The program has added several other foundries, but they share the shortcomings of negligible volume and a lack of capability to produce sub-12nm chips. This limits the program's relevance for critical next-generation systems like 6G-enabled Integrated Sensing and Communications, which require at 2-3 nm or smaller processes.[66]

RAMP-C: Bridging Modernization and Commercial Innovation

Launched under the CHIPS Act, RAMP-C leverages commercial foundries like Intel to prototype advanced nodes (e.g., 18A/2nm) for defense applications. Unlike the TSP's facility-based security approach, RAMP-C employs "quantifiable assurance" metrics using zero-trust concepts and attack-countermeasure analysis to assess risk quantitatively.[67] In 2023, Intel delivered test chips to Boeing and Northrop Grumman, but the transition from prototype to production remains challenging due to competing commercial priorities.[68] The program's data-centric methodology aims to ensure security for commercially procured dual-use chips, though these standards are still evolving.[69]

Microelectronics Commons: Advancing Lab-to-Fab Transitions

This $2B program, funded through the CHIPS Act, includes 33 projects across six technology areas, including AI hardware and electromagnetic warfare. It aims to facilitate the transition of microelectronics technologies from research and development to fabrication ("lab-

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[63] "List of Accredited Suppliers," Defense Microelectronics Activity, March 31, 2025, https://www.acq.osd.mil/asds/dmea/tapo/docs/tp/AccreditedSuppliers_31Mar2025.pdf.

[64] Laura A. Odell et al., *Supply Chain Risk in Leading-Edge Integrated Circuits*, D-21590, (Alexandria, VA: Institute for Defense Analyses, 2021), 1-2, https://www.ida.org/research-and-publications/publications/all/s/su/supply-chain-risk-in-leading-edge-integrated-circuits.

[65] "The Path to 1 Nanometer Chips and Beyond," IBM Research, December 5, 2022, https://research.ibm.com/blog/1nm-chips-vtfet-ruthenium.

[66] "Integrated Sensing and Communications for 6G," IEEE Communications Society, accessed October 27, 2024, https://ieeexplore.ieee.org/document/9376324.

[67] DODIG, "Evaluation of the DoD's Transition From a Trusted Foundry Model to a Quantifiable Assurance Method for Procuring Custom Microelectronics," May 4, 2022, https://www.dodig.mil/reports.html/Article/3019461/evaluation-of-the-department-of-defenses-transition-from-a-trusted-foundry-mode/.

[68] National Academies of Sciences, Engineering, and Medicine (U.S.) et al., eds., *Strategies to Enable Assured Access to Semiconductors for the Department of Defense*, Consensus Study Report (Washington, DC: National Academies Press, 2024), 67, https://doi.org/10.17226/27624.

[69] "DoD Releases Findings from Independent Panel Review of Microelectronics Quantifiable Assurance," U.S. Air Force, August 9, 2023, https://www.af.mil/News/Article-Display/Article/3488387/dod-releases-findings-from-independent-panel-review-of-microelectronics-quantif/#:~:text=The%20independent%20panel%20of%2027,off%2Dthe%2Dshelf%20components.

to-fab").[70] Furthermore, it will help mitigate the risks and will eventually grant access to the most cutting-edge microchips.

Secure Enclave: Enabling Dedicated Secure Production

Funded by a $3.5B CHIPS Act allocation, the Secure Enclave intends to establish a dedicated facility for sensitive projects with a single company: Intel. Announced in 2024, when Intel received funding to construct the secure manufacturing facility, the program targets extremely sensitive projects deemed insufficiently protected by TSP protocols.[71] Former Intel CEO, Pat Gelsinger, described it as an extension of existing DoD and Intelligence Community projects, suggesting it may serve as a production facility for RAMP-C designs.[72] Critics argue it is commercially unviable and risks underutilization, as defense demand alone cannot sustain commercial-scale production.[73]

DoDI 5200.44: Establishing Trusted Sourcing Mandate

This instruction establishes requirements for securing mission-critical functions and supply chains, particularly for microelectronics essential to defense applications.[74] It aims to mitigate risks associated with foreign dependencies and ensure components meet stringent security standards. However, its critical limitation is exempting most Commercial Off-The-Shelf (COTS) components from trusted sourcing requirements.[75] This creates significant vulnerabilities, as COTS products in defense systems bypass rigorous security assessments, exposing platforms to counterfeit components and common vulnerabilities and exposures that introduce side-channel attack risks.

Analysis - Systemic Challenges: Structural and Operational Vulnerabilities

While DoD uses various programs and policy frameworks to secure its microelectronics supply chain, structural and operational challenges persist. The following section examines these challenges in detail, highlighting the obstacles of fragmented governance, legacy system dependencies, and persistent security gaps that expose defense systems to operational and strategic risks.

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[70] Department of Defense, *National Defense Industrial Strategy: Implementation Plan for FY2025* (Washington D.C.: Department of Defense, 2024) 74. https://www.businessdefense.gov/docs/ndis/NDIS%20Implementation%20Plan_Revised_03182025_508.pdf.

[71] Christine Mui, "What's Really inside a Secret Chips Project," *POLITICO*, May 28, 2024, https://www.politico.com/newsletters/digital-future-daily/2024/05/28/whats-really-inside-a-secret-chips-project-00160233.

[72] Ibid.

[73] André Brunel, "Should the Pentagon Have Used Commerce Department Funds for Semiconductors?," *Defense News*, July 1, 2024, https://www.defensenews.com/opinion/2024/07/01/should-the-pentagon-have-used-commerce-department-funds-for-semiconductors/.

[74] Department of Defense, *Protection of Mission Critical Functions*, DoD Instruction 5200.44 (Washington D.C.: Department of Defense, 2012), 6, https://www.esd.whs.mil/portals/54/documents/dd/issuances/dodi/520044p.pdf.

[75] Ibid.

Fragmented Governance: Overlapping Authorities and Inconsistent Standards

The DoD's approach to microelectronics is shaped by multiple organizations with divergent missions and priorities, resulting in a lack of unified standards for semiconductor assurance and risk management. The Defense Microelectronics Activity (DMEA) manages the TSP, overseeing accreditation and implementing security measures such as chain of custody and tamper prevention.[76] The Office of the Under Secretary of Defense for Research and Engineering (OUSD(R&E)) sets strategic priorities for technology development, protection, and innovation, serving as the DoD's chief technology office and leading microelectronics research, prototyping, and transition efforts.[77] Meanwhile, the Office of the Under Secretary of Defense for Acquisition and Sustainment (OUSD(A&S)) is responsible for acquisition policy, sustainment, and modernization initiatives.[78] This decentralization of responsibilities leads to prioritization problems and slows the translation of objectives into operational outcomes.[79] The result is a patchwork of standards and requirements that complicates alignment within the DoD and the U.S. commercial base.[80]

Legacy System Neglect: Obsolescence and Supply Chain Gaps

Aging legacy systems present another major challenge for the DoD. Commercial electronics components typically have life cycles of five to seven years, while defense platforms often require reliable parts for more than two decades. This mismatch results in significant supply gaps and forces the DoD to rely on riskier procurement channels for obsolete or discontinued parts. A 2018 defense industrial base review found that 70 percent of electronic devices purchased by the DoD were already outdated before system fielding.[81] As a result, suppliers are often driven to secondary markets, increasing the risk of counterfeit semiconductors entering the supply chain. The DoD Inspector General has argued that the Trusted Supplier Program is "no longer viable for custom State-of-the-Art Microelectronics Procurement" because outdated requirements and commercial pressures restrict trusted foundries to increasingly obsolete technology.[82] This dynamic undermines operational readiness and increases the cost and complexity of maintaining secure and reliable defense systems.

Security Gaps: Globalization, Firmware Risks, and Overreliance on Foreign Production

The intricate and globalized nature of the semiconductor supply chain compounds security vulnerabilities. Companies that design chips domestically but rely on overseas partners for production expose sensitive design information and manufacturing know-how to adversaries. The over-reliance on foreign manufacturing, particularly in Taiwan, presents acute risks; more

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[76] "List of Accredited Suppliers," Defense Microelectronics Activity, 4.

[77] Heidi Shyu, "Technology Vision for An Era of Competition" (official memorandum, Washington, DC: Department of Defense, 2022) 3, https://www.cto.mil/wp-content/uploads/2022/02/usdre_strategic_vision_critical_tech_areas.pdf.

[78] Department of Defense, *Protection of Mission Critical Functions*, 2.

[79] U.S. Government Accountability Office, Defense Supply Chain Security, *GAO-24-112* (2024), 55.

[80] Odell, *Supply Chain Risk*, 9–11.

[81] Department of Defense, *2018 Industrial Capabilities Report to Congress* (Washington D.C.: Department of Defense, 2018), 45.

[82] DODIG, "Evaluation of the DoD's Transition From a Trusted Foundry Model," 7.

than 70 percent of ATP for defense systems occurs in East Asia.[83] Former Commerce Secretary Gina Raimondo warned that a Chinese seizure of chip producers via an invasion of Taiwan would have dramatic economic consequences for the United States.[84] Bloomberg has estimated that a war over Taiwan could cost the world economy over $10 trillion, or roughly 10 percent of global GDP.[85]

The increasing reliance on overseas production heightens the risk of disruptions and highlights vulnerabilities at both the hardware and firmware levels. While hardware assurance has traditionally focused on the provenance and integrity of physical components, modern hardware often includes embedded firmware that bridges hardware and software. Attacks on firmware can bypass hardware protections, undermining the presumed immutability of hardware because firmware, like software, can be exploited through design flaws or implementation errors. The trend toward "firmwarization," implementing hardware functions in firmware, blurs the distinction between hardware and software security. As a result, firmware should be subject to the same rigorous security standards as software, including open design scrutiny, restricted permissions, and minimized code complexity to reduce the likelihood of vulnerabilities.[86]

Recommendations - DoD-Centric Reforms for a Resilient Microelectronics Ecosystem

A suite of targeted reforms is required to address the systemic challenges described above. These reforms must leverage existing authorities, realign oversight mechanisms, and strengthen both the security and resilience of the defense microelectronics supply chain.

Centralized Governance: Creating a Unified Microelectronics Authority

To address the fragmented approach for procuring microelectronics, the DoD should establish a centralized Microelectronics Program Executive Office (PEO) under OUSD(A&S) that consolidates the Trusted Supplier Program, RAMP-C, and Microelectronics Commons initiatives.[87] A unified PEO would enforce a comprehensive roadmap that balances advanced node development with legacy system sustainment, ensure consistent application of security assurance levels across programs, and implement a risk-based approach to acquisition and validation.[88] By reducing bureaucratic barriers, the PEO would also facilitate greater industry participation.

Additionally, leveraging the Defense Innovation Unit (DIU) as a bridge between research and acquisition would enable cross-program collaboration. For example, DIU could coordinate joint validation protocols for commercial AI chips intended for secure enclaves, ensuring new

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[83] Department of Defense, *2024 Risk Assessment of Semiconductor Supply Chains* (Washington D.C.: Department of Defense, 2024), 22.

[84] Mui, "What's Really Inside a Secret Chips Project."

[85] Malcolm Scott, " A War Over Taiwan Is a $10 Trillion Risk," *Bloomberg News*, October 2024, https://www.bloomberg.com/news/newsletters/2024-01-09/economy-risks-latest-taiwan-war-would-cost-world-10-trillion.

[86] Lianying Zhao and David Lie, “Is Hardware More Secure Than Software?,” *IEEE Security & Privacy 18* no. 5 (September 2020): 8-17, https://doi.org/10.1109/MSEC.2020.2994827.

[87] U.S. Government Accountability Office, Defense Supply Chain Security, 55.

[88] National Academies of Sciences, Engineering, and Medicine, Strategies to Enable Assured Access to Semiconductors for the Department of Defense (Washington, DC: National Academies Press, 2024), 54–55.

technologies meet TSP accreditation and DFARS 252.246-7008 tamper-proofing requirements.[89] This approach would eliminate siloed efforts, reduce duplicative testing, and create more consistent security standards across the Department.

Security Enforcement: Implementing Comprehensive Protection Measures

The DoD's heavy reliance on COTS components—with 58% sourced from global supply chains—creates significant vulnerabilities to counterfeit infiltration and supply chain manipulation. To address these vulnerabilities, the DoD should implement a multi-layered security approach.

First, a mandatory testing framework should require compliance with the National Institute of Standards and Technology's platform resiliency guidelines (NIST SP 800-193) for all microelectronics in critical systems, including COTS components. This framework should incorporate Physically Unclonable Functions (PUFs), physical entities embedded in a semiconductor device that leverage inherent, uncontrollable, and random physical variations from manufacturing to create a unique, unclonable "fingerprint" for the device. PUFs have emerged in the last decade as some of the most cost-effective security primitives for hardware trust anchors.[90] While PUFs are not a silver bullet, they can be effectively used for counterfeit prevention, detection of physical tampering, and runtime verification protocols for firmware integrity monitoring.[91]

Second, supply chain visibility must be enhanced by expanding the National Industrial Security Program to include Tier 2 and Tier 3 suppliers implementing zero-trust principles throughout the supply network.[92] This would enable real-time monitoring of assembly, ATP processes, verification of firmware update chains, and traceability of components from design through deployment.

Third, developing secure design tools should be accelerated through partnerships with academic institutions. For instance, Purdue University's SCALE program demonstrated a 40 percent reduction in satellite subsystem vulnerabilities through its "Trusted IC" initiative model that could be expanded to other defense applications.[93] For legacy systems, the DoD should mandate the adoption of PUFs to authenticate components without requiring costly redesigns.[94] These hardware-specific cryptographic signatures provide a cost-effective means of securing existing systems against tampering and counterfeiting.

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[89] Defense Acquisition Regulations System, DFARS 252.246-7008 (April 2025).

[90] Sergio Vinagrero et al., "SRAM-Based PUF Readouts," Scientific Data 10, no. 1 (2023): 333, https://doi.org/10.1038/s41597-023-02225-9.

[91] Yu Qin et al., "RIPTE: Runtime Integrity Protection Based on Trusted Execution for IoT Device," Security and Communication Networks 2020, no. 1 (2020): 8957641, https://doi.org/10.1155/2020/895764.

[92] Defense Science Board, Cybersecurity of the Defense Industrial Base (2017), 29.

[93] Purdue University, Trusted IC Initiative Annual Report (2024), 12.

[94] Mohammad Ebrahimabadi et al., *Countering PUF Modeling Attacks through Adversarial Machine Learning* (Tampa, FL: IEEE, 2021) 356–61, https://ieeexplore.ieee.org/document/9516754/.

Ally Integration: Building Resilient Multinational Supply Networks

The DoD's reliance on overseas manufacturing introduces acute geopolitical supply-chain risks.[95] A 2024 DoD assessment projected that a Chinese blockade of Taiwan could disrupt 85 percent of defense-grade microelectronics production within six weeks, potentially crippling critical defense programs such as the F-35 and Patriot missile systems.[96]

To mitigate these risks, the DoD should pursue a two-pronged approach. First, it should work with international partners to co-fund an advanced packaging facility for defense purposes with allied nations including Japan, Malaysia, and South Korea. This facility would focus on radiation-hardened chips and other defense-specific applications, creating geographic diversity to protect the DoD semiconductor supply chain during a Taiwan contingency. Second, the DoD should work with allies to align export controls and security protocols, facilitating the secure exchange of process design kits (PDKs) and other critical intellectual property. Building upon Japan's 2024 chip packaging resilience initiative, which aims to grow Japan's domestic ATP capabilities, these partnerships would establish common verification standards and mutual recognition of security certifications.

Issue Wrap-Up

By unifying oversight, strengthening enforcement, and deepening integration with allies, the DoD can better protect its technological edge and maintain operational readiness in an increasingly contested global environment. Ultimately, U.S. defense systems' enduring security and competitiveness will rely on the Department's ability to adapt its microelectronics strategy to meet current and future challenges.

CONCLUSION

As Great Power Competition continues to dominate global geopolitics, semiconductor production capabilities have never been more important. This paper's recommendations across critical inputs, workforce, advanced packaging, and security demand focus, sustained investment, and national will. However, they will also profoundly enhance the United States' economic health, national security, global competitiveness. Collectively, they represent an important "waking up," shifting the momentum back towards a resurgent United States that is ready to lead in this crucial industry.

As the DoD considers how it can strengthen access to microelectronics and reduce risk, future study should evaluate gaps in the specific types of semiconductors it procures, the role that internal DoD educational institutions ranging from technical schools to Defense Acquisition University can play, and how trade policy is impacting procurement of microelectronics for defense.

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[95] Department of Defense, *Risk Assessment of Semiconductor Supply Chains*, 22.
[96] Ibid., 72.

APPENDIX A: THE TRANSFORMATIVE IMPACT OF ARTIFICIAL INTELLIGENCE ON SEMICONDUCTOR MANUFACTURING

Adopting AI-driven semiconductor manufacturing techniques benefits the United States by ensuring a stable supply of advanced electronics used in everyday devices. It also fortifies U.S. defense capabilities by delivering high-performance chips for military systems and critical infrastructure. This appendix summarizes the industry's current opportunities, persistent obstacles to AI adoption in chip manufacturing, and adversarial considerations.

Strategic Advantages of AI Integration

Aspect	AI Application & Benefits	Examples & Details
Predictive Maintenance	User sensor data and machine learning to forecast equipment failures, reducing downtime and maintenance costs; enhances supply chain security.[97]	TSMC and GlobalFoundries reported significant reductions in unplanned downtime and costs after deploying AI-based monitoring systems.[98] These improvements help to ensure reliable production for critical applications.
Quality Control & Defect Detection	AI-powered computer vision inspects wafers and chips at microscopic levels, identifying defects with over 99% accuracy, reducing failure risks in critical military hardware.[99]	Intel and TSMC have implemented high-speed AI inspection tools analyzing thousands of wafer images per hour.[100] Military systems such as F-35, and F-22 rely on TSMC and Intel[101] chips for operational reliability.[102, 103]
Chip Design & Electronic Design Automation (EDA)	AI tools optimize layout, power, and signal integrity, reducing design cycle times by up to 30%, enabling rapid development of	Companies like Synopsys have integrated AI into their EDA workflows to develop chips for AI, automotive electronics, and 5G

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[97] David Park, “A Blueprint for Semiconductor Manufacturing Success with AI/ML Adoption,” Tignis, April 23, 2024, https://tignis.com/2024/04/22/transforming-semiconductor-manufacturing-with-ai-and-ml-2/.

[98] Harsh Savani, “AI in Semiconductors Industry: Innovations Ahead [2025],” December 31, 2024, https://www.aegissofttech.com/insights/ai-in-semiconductor-industry/.

[99] “The Role of Artificial Intelligence in Semiconductor Manufacturing | ManufacturingTomorrow,” accessed May 7, 2025, https://manufacturingtomorrow.com/content.php?post=23450.

[100] “The Role of Artificial Intelligence in Semiconductor Manufacturing | ManufacturingTomorrow.”

[101] “F-22 Avionics Designers Rely on Obsolescent Electronics, but Plan for Future Upgrades,” Military Aerospace, May 1, 2001, https://www.militaryaerospace.com/computers/article/16710716/f-22-avionics-designers-rely-on-obsolescent-electronics-but-plan-for-future-upgrades.

[102] Sujai Shivakumar and Charles Wessner, “Semiconductors and National Defense: What Are the Stakes?,” June 8, 2022, https://www.csis.org/analysis/semiconductors-and-national-defense-what-are-stakes.

[103] “F-22 Avionics Designers Rely on Obsolescent Electronics, but Plan for Future Upgrades.”

	complex, application-specific chips.[104]	applications faster and more efficiently.[105]
Supply Chain Management	AI models forecast demand and optimize inventories, making supply chains more resilient and reducing costs.[106]	Samsung’s AI tools have helped cut over $1 billion in annual inventory costs, improving responsiveness to market fluctuations and disruptions.[107]
Energy Efficiency & Sustainability	AI identifies energy savings by optimizing manufacturing equipment, reducing resource waste, and improving process efficiency.[108]	Applied Materials achieved 35% reduction in energy use for specific etching processes through AI-driven process optimization, supporting sustainability goals.[109]

Obstacles to Realizing AI’s Full Potential

Companies are slowly adapting AI into semiconductor manufacturing; however, they are encountering various obstacles that make widespread implementation challenging.

High Implementation Costs and Technical Complexity

AI integration in semiconductor manufacturing is costly and complex, posing challenges for smaller manufacturers.

Data Security and Intellectual Property Risks

Robust cybersecurity is vital to protect sensitive data as AI becomes more integrated into semiconductor manufacturing.

Talent Shortages and Workforce Transition

The industry faces a talent gap, with many workers needing retraining for AI-driven systems, as over 60% of inspection roles are now automated, requiring new skills.

Integration with Legacy System

Retrofitting legacy semiconductor facilities for AI integration is costly and disruptive, with ongoing challenges in ensuring compatibility with existing equipment.

110, 111

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[104] Team DigitalDefynd, “10 Ways AI Is Being Used in Chip Manufacturing [2025],” DigitalDefynd, June 8, 2024, https://digitaldefynd.com/IQ/ai-in-chip-manufacturing/.

[105] Ibid.

[106] “Semiconductor Industry Outlook 2025," Infosys Knowledge Institute,” accessed May 7, 2025, https://www.infosys.com/iki/research/semiconductor-industry-outlook2025.html.

[107] Team DigitalDefynd, “10 Ways AI Is Being Used in Chip Manufacturing [2025].”

[108] “The Role of Artificial Intelligence in Semiconductor Manufacturing | ManufacturingTomorrow.”

[109] “Vistara,” Applied Materials, accessed May 7, 2025, https://www.appliedmaterials.com/us/en/product-library/vistara.html.

[110] “The Intersection of AI and Semiconductors,” Microchip USA, March 15, 2025, https://www.microchipusa.com/industry-news/the-intersection-of-ai-and-semiconductors-advancements-implications-and-future-opportunities.

[111] Harsh Savani, “AI in Semiconductors Industry: Innovations Ahead [2025],” Aegis Softtech, December 31, 2024, https://www.aegissofttech.com/insights/ai-in-semiconductor-industry/.

Adversarial Considerations

The United States risks losing its technological superiority if it does not match China's AI-driven advancements in semiconductor manufacturing. Huawei's ultrafast 6G smart factory claims to operate at one terabit per second and have zero production latency. This means that even milliseconds of delay on a traditional network do not exist. Zero latency eliminates this bottleneck completely. The instant data exchange allows robotic AI-driven systems to predict maintenance needs before breakdowns and adapt supply chains to customer demand.[112] While there is limited direct evidence detailing the extent of Huawei's use of AI in manufacturing process, it is plausible and increasingly likely that AI is playing a role in helping Huawei and its partner SMIC to design and mass produce 7nm chips using deep ultraviolet (DUV), which is pushing the technology beyond what experts believed was practical or economically viable, with the purpose of countering U.S. restrictions.[113] If the United States does not accelerate its own AI-driven chip manufacturing capabilities, it risks ceding leadership to China in this realm, undermining national security in an era where dominance in semiconductors and AI is directly linked to military and economic power.[114]

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[112] Revo Now, "Huawei's 6G Smart Factory: Zero Latency Revolution," video, February 28, 2025, 25:10 https://www.youtube.com/watch?v=ovCUwK_8gyQ.

[113] "Huawei's First Attempt to Make Its Own "7nm High-End Chips" to Create a One-Stop AI Supply Chain?," video, May 7, 2025, https://www.youtube.com/watch?v=gep3yxr0Ufg. Note: translated by student Amy Chou.

[114] Shivakumar, "Semiconductors and National Defense: What Are the Stakes?"

APPENDIX B: WARGAMING IN THE SEMICONDUCTOR INDUSTRY - STRATEGIC PREPAREDNESS AGAINST SUPPLY CHAIN DISRUPTIONS

Introduction

Think tanks and the private sector are increasingly employing wargaming to assess vulnerabilities and develop strategies to mitigate risks within the semiconductor supply chain. The implications for national security are profound, as semiconductors are critical components in numerous defense systems and underpin broader economic stability. The federal government and DoD should follow suit and conduct a thorough wargame to understand the national security implications of the semiconductor supply chain on the US and its allies.

Why Wargaming is Important

a. Scenario Simulation: Wargaming would enable DoD and the private sector to simulate various disruption scenarios, such as geopolitical tensions, natural disasters, or cyberattacks. By modeling these scenarios, stakeholders can evaluate the potential impacts on military operations and supply chains, allowing for proactive risk management.[115]

b. Strategic Decision-Making: Insights gained from wargaming shape strategic decision-making by revealing the need for increased domestic semiconductor manufacturing capabilities to reduce reliance on foreign suppliers, which is crucial for national security.[116]

c. Collaboration and Information Sharing: Wargaming facilitates collaboration between the DoD, private sector companies, and allied nations. By involving industry partners in simulations, the DoD can gain valuable insights into commercial practices and technological advancements, fostering a more resilient semiconductor ecosystem.[117]

d. Anticipating Adversarial Actions: The DoD can use wargaming to anticipate and prepare for potential adversarial actions that target semiconductor supply chains. This proactive approach enables the development of countermeasures and enhances the security of critical technologies.[118]

e. Policy Development: The outcomes of wargaming exercises produce national policies aimed at strengthening the semiconductor industry and enhancing supply chain resilience. By understanding the implications of various scenarios, policymakers can craft regulations and initiatives that bolster national security.

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[115] Sebastian J. Bae, “How Can Wargaming Improve Government Response to Catastrophic Events?” RAND Corporation, May 29, 2020, https://www.rand.org/pubs/commentary/2020/05/how-can-wargaming-improve-government-response-to-catastrophic.html.

[116] U.S Government Accountability Office, “Defense Analysis: Additional Actions Could Enhance DOD's Wargaming Efforts,” April 24, 2023, https://www.gao.gov/products/gao-23-105351.

[117] Kelly E. Pecotte, *Interorganizational Wargaming as a Tool for Building Collaborative Partnerships and Improving Future Senior Level Civil-Military Relations* (Quantico, VA: U.S. Marine Corps Command and Staff College, 2021), https://apps.dtic.mil/sti/trecms/pdf/AD1178146.pdf.

[118] U.S. Government Accountability Office, “Defense Analysis.”

Wargame Scenarios

Specialization within the semiconductor industry necessitates an understanding of supply chain interruptions. Think tanks and private industry often conduct wargames and produce unclassified analyses of their results to map risks, vulnerabilities, identify anticipatory actions, and enable decision making.

Thank Tank, 2022:

RAND conducted a tabletop exercise (TTX) with senior leaders from the executive and legislative branches and a variety of industry leaders to assess geopolitical implications of Taiwan's semiconductor dominance. RAND's TTX exposed inherent weaknesses in the US's strategic semiconductor positioning and was found to be at a disadvantage to China during both peacetime and contingency scenarios. Their study produced key findings and recommendations highlighting that most TTX participants were unaware of the vulnerabilities generated by Taiwan's semiconductor dominance and the need for the US government to improve its analysis and understanding of the supply chain. [119]

Private Sector, 2023 and 2024:

Willis Towers Watson (WTW), a leader in the insurance and risk management industry, conducted an extensive survey to identify emerging threats to the semiconductor industry.[120] Their results found that the primary disruption concerns are raw material shortages, utility interruptions, and logistics challenges caused, or exacerbated, by climate change, cyber threats, and geopolitical factors.[121] Both companies cite a concern about insurance companies failing to provide sector-specific insurance solutions to protect affected firms against operational disruptions.[122] Firm failure in this industry would exacerbate any disruptive force and have a long-term impact on the global economy.

Future of Wargaming

These examples highlight the utility of wargaming within the semiconductor industry. However, the DoD's presence is noticeably absent in these examples. Wargaming semiconductor supply chain interruptions from a defense standpoint is a critical component to a holistic understanding of its impact on national security. Given RAND TTX's and WTW's findings, a federal-level wargame including all elements of national power (diplomatic, informational, military, and economic) should be held to develop a comprehensive understanding of the semiconductor supply chain. This wargame should endeavor to identify critical vulnerabilities, develop mitigating strategies, and create a strategic path to ensure economic prosperity and defense superiority.

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[119] Bradley Martin et al, *Supply Chain Interdependence and Geopolitical Vulnerability* (Santa Monica, CA: RAND Corporation, 2023), 31, https://www.rand.org/pubs/research_reports/RRA2354-1.html

[120] Willis Tower Watson, *2023 Semiconductor Supply Chain Risk Report* (London: WTW, 2023), https://www.wtwco.com/en-ph/insights/2023/05/2023-semiconductor-supply-chain-risk-report.

[121] WTW, *2023 Semiconductor Supply Chain Risk Report*.

[122] WTW, *2023 Semiconductor Supply Chain Risk Report*.

ANNEX 1: USE OF ARTIFICIAL INTELLIGENCE

ACADEMIC DECLARATION

1. All AI-generated outputs were critically reviewed, edited, and integrated by the authors, who take full responsibility for the accuracy and integrity of the final manuscript.

2. We acknowledge the use of Grammarly in helping us review our writing at the final stage of preparing our paper submission. We used the following features: Clarity and correctness. We critically reviewed the feedback generated by Grammarly and, based on this, revised the writing using our own words and expressions.

3. We acknowledge using Perplexity AI to create an initial framework for this paper by synthesizing common themes and generating an outline from four individual reference papers.

4. We acknowledge the use of Perplexity AI to assist with advanced academic editing tasks. Specifically, Perplexity was used to:
    a. Verify numerical data, statistics, and experimental results against cited sources.
    b. Flag inconsistencies in datasets, methodological descriptions, or result interpretations.
    c. Identify unsupported claims lacking evidentiary backing.
    d. Evaluate the credibility of all references using the CRAAP criteria (Currency, Relevance, Authority, Accuracy, Purpose).
    e. Highlight non-peer-reviewed sources needing replacement and flag sources from potentially predatory journals.
    f. Identify citation gaps, including statements requiring citations, improper paraphrasing, missing seminal works, and excessive self-citation or citation bias

SPECIFIC PROMPTS AND RESPONSES

Generative AI platform used: Perplexity

Prompt used: "Top Five Outsourced Assembly and Testing (OSAT) Companies in the World"

The global OSAT (Outsourced Semiconductor Assembly and Test) industry is dominated by a handful of large players, primarily based in Taiwan, the United States, and China. The top five companies, based on recent market share, revenue, and industry consensus, are:

Rank	Company Name	Headquarters	Estimated Market Share (2024–2025)

1	ASE Technology Holding Co., Ltd.	Kaohsiung, Taiwan	~30%
2	Amkor Technology, Inc.	Tempe, Arizona, USA	~14%
3	JCET Group Co., Ltd. (Jiangsu Changjiang Electronics Technology)	Shanghai, China	~12%
4	Powertech Technology Inc. (PTI)	Hsinchu, Taiwan	~8%
5	Tongfu Microelectronics Co., Ltd.	Suzhou, China	~5%

Company Overviews

ASE Technology Holding Co., Ltd.

- The world's largest OSAT provider, with a comprehensive portfolio spanning advanced packaging, system-in-package (SiP), and testing services[1][2][3].
- Formed through the merger of ASE and Siliconware Precision Industries (SPIL), further consolidating its leadership position[4].

Amkor Technology, Inc.

- The largest OSAT provider outside Asia and the second-largest globally.
- Known for advanced packaging technologies, including wafer-level packaging and high-density solutions for 5G, AI, and automotive applications[1][2][3].

JCET Group Co., Ltd.

- The top OSAT provider in China, offering a wide range of assembly and testing services, including advanced packaging and SiP solutions.
- Strong R&D and a growing international presence[1][2][3].

Powertech Technology Inc. (PTI)

- Specializes in advanced memory packaging and testing, particularly for DRAM and NAND flash.
- Recognized for technical innovation and strong partnerships with major memory manufacturers[2][5][3].

Tongfu Microelectronics Co., Ltd.

- A leading Chinese OSAT company, known for cost-effective operations and a strong domestic market presence.
- Focuses on both traditional and advanced packaging services[3].

Industry Context

These five companies consistently rank at the top in terms of revenue, market share, and technological capabilities across multiple industry reports and market analyses[1][2][5][4][3]. The OSAT industry is highly competitive and fragmented, but these leaders have distinguished themselves through scale, innovation, and strategic partnerships.

Other notable OSAT companies just outside the top five include Siliconware Precision Industries (now part of ASE), King Yuan Electronics Co. (KYEC), Huatian Technology, and ChipMOS Technologies[2][5][4][3].

Summary Table

Company Name	Headquarters	Key Strengths
ASE Technology Holding Co., Ltd.	Taiwan	Scale, innovation, advanced packaging
Amkor Technology, Inc.	USA	Advanced packaging, global reach
JCET Group Co., Ltd.	China	R&D, domestic and global expansion
Powertech Technology Inc.	Taiwan	Memory packaging expertise
Tongfu Microelectronics Co., Ltd.	China	Cost efficiency, strong domestic presence

These companies form the backbone of the global semiconductor packaging and testing supply chain, supporting leading integrated device manufacturers (IDMs) and fabless semiconductor companies worldwide[1][2][3].

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1. https://techovedas.com/top-10-osat-outsourced-semiconductor-assembly-and-test-companies-in-2024/

2. https://evertiq.com/news/51003
3. https://www.linkedin.com/posts/kumar-priyadarshi-b0a2a7a2_top-10-osat-outsourced-semiconductor-assembly-activity-7312043723415072769-EOep
4. https://www.verifiedmarketresearch.com/blog/top-osat-companies-2/
5. https://www.mordorintelligence.com/industry-reports/osat-market/companies

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Generative AI platform used: Perplexity

Prompt used: "How much of the DoD RDT&E budget goes to microelectronics?"

DoD RDT&E Funding for Microelectronics in FY2025

The Department of Defense allocates a portion of its Research, Development, Test, and Evaluation (RDT&E) budget to microelectronics programs. For FY2025, the main microelectronics-related funding lines are:

- **Defense Microelectronics Activity (DMA):** $137.2 million (down from $144.7 million in FY2024 and $201 million in FY2023)
- **Trusted & Assured Microelectronics (T&AM):**
    - Advanced Component Development & Prototype: $593.6 million (down from $624.3 million in FY2023)
    - System Development & Demonstration: $150.4 million (down from $245.4 million in FY2023)
- **Microelectronics Commons:** No new DoD funding is allocated for FY2025, as this program is funded separately at $400 million per year through the CHIPS for America Defense Fund for FY2023–2027[1].

Summary Table: DoD Microelectronics RDT&E Funding (FY2025)

Program/Line	FY2025 Funding (USD)
Defense Microelectronics Activity	$137.2 million
Trusted & Assured Microelectronics (ACD&P)	$593.6 million
Trusted & Assured Microelectronics (SD&D)	$150.4 million
Microelectronics Commons (DoD RDT&E)	$0 (CHIPS Act funds)

Total (excluding CHIPS Act)	**$881.2 million**

- **Total DoD RDT&E for microelectronics in FY2025 is approximately $881 million**, not including the $400 million per year from the CHIPS Act Defense Fund, which supports the Microelectronics Commons program[1].

Context

- This funding represents a small fraction of the total DoD RDT&E budget, about $141 billion for FY2025[2][1].
- The microelectronics budget has seen reductions in some lines compared to previous years, reflecting shifting priorities and the impact of external funding streams like the CHIPS Act[1].

In summary:

Roughly $881 million of the DoD’s FY2025 RDT&E budget is directly allocated to microelectronics programs, with an additional $400 million per year for Microelectronics Commons provided via the CHIPS Act rather than the core DoD RDT&E budget[1].

⁂

1. https://www.digitimes.com/news/a20240313VL203/us-2025-defense-budget-ic-manufacturing.html
2. https://www.defense.gov/News/Releases/Release/Article/3703410/department-of-defense-releases-the-presidents-fiscal-year-2025-defense-budget/

Generative AI platform used: Perplexity

Prompt used: “Make me a table that summarizes the 2D, 2.5D, 3D, and 3DHI technologies over time”

Technology	Era of Adoption	Structure & Integration	Key Features & Advantages	Challenges & Limitations	Typical Applications

2D IC	1960s–present	Single die, planar (flat) layout	Mature, low cost, easy thermal management, high yield	Interconnect bottlenecks, scaling limits	General electronics, CPUs, SoCs
2.5D IC	2010s–present	Multiple dies side-by-side on a silicon interposer (no vertical stacking)	Heterogeneous integration, high bandwidth, flexibility, easier thermal handling	Interposer cost, design complexity	GPUs, AI accelerators, HBM memory, networking ASICs
3D IC	2010s–present (R&D in 1980s)	Multiple dies stacked vertically, connected by TSVs or hybrid bonding	Shorter interconnects, reduced power, higher density, enables true vertical integration	Thermal issues, yield, design/test complexity, TSV overhead	HMC, NAND flash, image sensors, advanced SoCs
3DHI (3D Heterogeneous Integration)	2020s–emerging	Stacks multiple dies of different types/processes (logic, memory, analog, RF) in 3D	Combines best process nodes, enables system-in-package, security, ultimate integration	Thermal, yield, complex design, supply chain	Defense, advanced AI, high-performance computing, secure systems

Notes:

- **2.5D ICs** use an interposer for side-by-side die placement, providing high interconnect density without the thermal challenges of vertical stacking[1].
- **3D ICs** achieve higher integration by stacking dies, reducing wire length and power, but face thermal and yield hurdles[2][3][1].
- **3DHI** is an emerging approach that leverages 3D stacking for heterogeneous system integration, targeting advanced and secure applications[2][4][5].
- The timeline reflects when each technology became prominent in commercial or research use; 3DHI is still in early adoption.

This table provides a concise historical and technical comparison of 2D, 2.5D, 3D, and 3DHI integration technologies.

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1. https://www.einfochips.com/blog/2-5d-3d-ics-new-paradigms-in-asic/
2. https://en.wikipedia.org/wiki/Three-dimensional_integrated_circuit
3. https://semiengineering.com/knowledge_centers/packaging/advanced-packaging/3d-ics/
4. https://www.sciencedirect.com/science/article/pii/S2772671122000249
5. https://semiengineering.com/knowledge_centers/manufacturing/packaging/advanced-packaging/heterogeneous-integration/

Generative AI platform used: Perplexity

Prompt used: "What specific projects are funded under the Microelectronics Commons?"

Specific Projects Funded Under the Microelectronics Commons

The Department of Defense's Microelectronics Commons program, funded by the CHIPS and Science Act, has awarded funding to **33 projects** across six critical technology areas. These projects are distributed among eight regional hubs and are designed to accelerate domestic microelectronics prototyping, manufacturing, and workforce development[1][2][3].

Technology Areas and Example Projects

Technology Area	Number of Projects	Total Funding (approx.)	Example Projects/Focus
5G/6G Wireless	5	$42 million	Prototyping high-frequency wireless systems, scalable MIMO arrays[4][2]
Commercial Leap-Ahead	7	$38 million	Advancing high-power AlGaN systems, next-gen commercial semiconductor tech[4][2]
Artificial Intelligence (AI)	7	$42 million	AI hardware accelerators, secure AI processing modules[2]
Electromagnetic Warfare (EW)	6	$51 million	Microelectronics for EW applications, resilient RF systems[2][3]
Quantum Technology	4	$32 million	Hybrid quantum-photonic integrated circuits[4][2]
Secure Edge/IoT Computing	4	$25 million	Secure GPU processing modules, edge computing for tactical use[2]

Cross-Hub Enablement Solution	1	$39 million	Shared access to electronic design automation (EDA) tools and cloud resources[1][2][5]

Notable Project Examples by Hub

- **Midwest Microelectronics Consortium (MMEC) Hub**: Five projects, including electromagnetic warfare, 5G/6G applications, AI hardware, and secure edge/IoT computing. Example: "Validated GPU Based Secure Processing Module" for secure tactical edge operations[2][3].
- **Silicon Crossroads Microelectronics Commons (SCMC) Hub**: Four projects, such as secure edge/IoT computing, AI hardware, and EW applications[2].
- **Southwest Advanced Prototyping (SWAP) Hub**: Five projects, including 5G/6G, AI hardware, commercial leap-ahead, and secure edge/IoT[2].
- **Northeast Microelectronics Coalition (NEMC) Hub**: Projects include "Advancing DoD High Power Systems: Transition of High Al% AlGaN from Lab to Fab" (commercial leap-ahead) and "Wideband, Scalable MIMO arrays for NextG Systems" (5G/6G), as well as quantum technology projects like "Community-driven Hybrid Integrated Quantum-Photonic Integrated circuits (CHIQPI)"[4].

Program Goals

The Microelectronics Commons projects aim to:

- Accelerate the transition of microelectronics technologies from lab to fab
- Strengthen domestic prototyping and manufacturing
- Grow the U.S. semiconductor talent pipeline
- Enable next-generation defense and commercial systems[1][3]

Additional Notes

- The Cross-Hub Enablement Solution ($39 million) provides all hubs with equal access to critical EDA tools and cloud computing for chip design and prototyping[2][5].
- The program is structured to ensure collaborative innovation across industry, academia, and government partners[6][3].

In summary:

The Microelectronics Commons funds 33 projects across six key technology areas, with specific initiatives ranging from secure AI hardware and quantum circuits to advanced 5G/6G systems and electromagnetic warfare applications, all distributed among eight regional hubs and supported by shared design and prototyping infrastructure[1][4][2].

⁂

1. https://www.meritalk.com/articles/dod-sets-269m-funding-for-33-microelectronics-tech-projects/
2. https://insidedefense.com/share/222384
3. https://www.prnewswire.com/news-releases/the-mmec-receives-microelectronics-commons-project-awards-302253508.html
4. https://news.mit.edu/2024/microelectronics-projects-awarded-chips-science-act-funding-1001
5. https://www.meritalk.com/articles/pentagon-boosts-microelectronics-hubs-with-160m-chips-act-funding/

https://microelectronicscommons.org

Generative AI platform used: Microsoft Copilot

Prompt used: "Please prepare a 1 paragraph executive summary of this paper." (Using a complete version of the paper from 9 May 2025)

This paper analyzes the critical challenges facing the U.S. semiconductor industry and provides strategic recommendations to strengthen national competitiveness, security, and technological leadership. It examines four key areas: securing critical inputs, addressing workforce shortages, advancing packaging technologies, and fortifying defense microelectronics. The paper highlights vulnerabilities in the supply chain, the urgent need for domestic talent development, and the importance of reshoring advanced semiconductor production. It also explores how AI-driven manufacturing, wargaming exercises, and policy interventions can mitigate risks and enhance resilience. The proposed solutions, including targeted investments, regulatory reforms, and international collaboration, aim to ensure the United States maintains its semiconductor leadership in the face of growing global competition, particularly with China.